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Seven Level Multilevel Inverter With Reduced Number of Switches Configured With Boost Converters for Standalone PV Systems

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Abstract. Multilevel inverters (MLI) are designed to handle the medium voltage and high-power requirements of industrial plants or power systems. The traditional structure of the MLI topologies necessities additional switches and limits its wide range of use. This research describes the work done on a single-phase 7-level MLI with a reduced number of switches (RSMLI) topology used in a standalone photovoltaic (PV) system. The proposed RSMLI structure integration with three individual PV arrays controlled by fuzzy logic maximum power point tracking (FL-MPPT) technique and three boost converters instead of a separate direct-current (DC) source. The proposed MLI uses a smaller number of controlled switches, a lower number of PV arrays, and fewer diodes. Furthermore, a simple unipolar Phase Disposition Pulse Width (PD PWM) Modulation technique was used instead of the conventional high-cost bipolar PWM technique. The performance of the proposed inverter was tested under different solar irradiance levels and load conditions in the simulation using Matlab/Simulink. The results show that the proposed seven-switches MLI presents a 7-level at the output, and it offers good total harmonic distortion (THD) content in the output voltage where a THD value of 18.17% was obtained without filter

Keywords. Boost converter, multilevel inverter, reduced number of switches, standalone photovoltaic system, phase disposition PWM, seven level inverter

INTRODUCTION

Because of rising concerns in many nations throughout the world, renewable energy (RE) has gained a lot of attention in recent decades. RE sources have been extensively proposed as a solution to the problem of expanding electrical energy demand while limiting the negative impact of burning fossil fuels [1-3]. Photovoltaic cells (PV) collected RE has considerably contributed to the decrease of harmful emissions. However, different approaches of using PV systems to supply adequate PV power to loads or the grid are provided, which will influence installation costs and system efficiency [4]. Furthermore, the PV systems characteristics are considered nonlinear as a result of the influence of weather conditions. For this reason, a maximum power point tracking (MPPT) controller is utilized to enhance performance and boost PV efficiency in a variety of weather circumstances [5-9]. Many MPPT methods are used for the standalone PV systems to achieve the maximum power such perturb and observe (P&O), incremental conductance (IC) method, fuzzy logic (FL) method, neural network, particle swarm optimization based MPPT [10-13].

DC/AC converters are critical components in the operation of a PV system since they provide AC voltage from the PV system [14-16]. Traditional inverters used for standalone applications have significant downsides, such as increased total harmonic distortion (THD) and the need for a large filter size [17-20]. Nowadays, the PV system-based multilevel inverter (MLI) architecture has received a lot of attention in medium-voltage high power applications because it has more benefits than traditional inverters, such as lower THD content and lower switching losses [21].

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Moreover, For DC-to-AC conversion, three basic MLI topologies have been suggested and reviewed: cascaded H-bridge (CHB) MLI, neutral point clamped (NPC) MLI, and flying capacitor (FC) MLI topologies [22-24]. However, these topologies have significant limitations, such as the fact that NPC MLI requires a bigger number of switches and diodes to produce the appropriate 3, 5, and 7 levels voltage. For these reasons, numerous MLI with fewer switches are presented in the literature to minimize the number of switches.

Hari P. et al [25] proposed a new reduced switches (RSMLI) topology based minimum number of PWM carries and reduced number of switches. The presented PWM technique was implemented with only three carries to trigger the switches and generate 7 and 13-level output voltage. Also, the studied PWM technique can be applied to any RSMLI circuit. The simulation and experimental results show that the proposed technique can reduce the THD content in the output voltage and improve the performance of the inverter. Authors in [26] were proposed nine level RSMLI for single-phase AC application. The proposed inverter was controlled using sinusoidal PWM technique to obtain the suitable PWM signals for the inverter's switches. Besides, the inverter was designed with nine switches and two diodes and it produce 9-level output voltage.

Shivam P. G et al [27] presented hybrid symmetrical MLI with minimum number of switches. The designed inverter was implemented in experiment with only 7 switches to generate seven level output voltage. The presented inverter offers reduced no. of switches, diodes, dc voltage sources when it compared with conventional MLI topologies. As a result, the performance, efficiency and cost of the implementation were improved. Also, authors in [28] proposed a modified RSMLI inverter topology using three dc sources, seven switches, and two diodes. The modified RSMLI was validated by simulation using MATLAB/Simulink software. The results show that the proposed topology provides reduced number of switches, and reduced no. of gate drivers which are minimized the overall cost of the implementation and then minimize the weight and size of the circuit.

Authors in [29] were proposed a single phase MLI with the fewest number of switches. The study's goal is to minimize the number of switches utilized in standard H-bridge-based boost converters for PV systems. The authors created a novel MLI-based H-bridge with only four DC sources and 14 switches. This architecture provides a 7 and 13-level output voltage with a low THD value. The biggest issue with the number of switches is that the topology still has 14 controlled switches.

For this reason, this paper aims to design a 7-level RSMLI topology configuration with DC/DC boost converters used in standalone PV systems. The main contribution of this work is to propose a MLI inverter circuit with reduced number of controlled switches, DC sources, and no. of gate drivers. In addition, a output voltage with 7-levels was obtained using only seven controlled switches. The proposed topology was applied using multi-DC/DC boost converters that integrated with individual PV array to produce the required DC voltage instead of conventional separate DC sources. The disposition (DP) PWM technique was used to control the switches of the suggested inverter. Each PV array was controlled using Fuzzy logic MPPT method to enhance the performance and increase its efficiency under different weather conditions.

This research was organized as follows: Section 2 reports reduced switches MLI topology. Section 3 presents the system detailed modeling. Section 4 presents the simulation results and discussion while section 5 introduces the conclusion.

REDUCED SWITCHES MLI TOPOLOGY

To attain the same levels without increasing the number of semiconductor devices, a new contemporary MLI architecture based on a reduced number of switches was created [25,26]. Various topologies are created and described in the literature to minimize the number of switches while achieving the same output voltage level with the lowest THD content, such as in [29,30].

However, MLI topologies with fewer switches that function with individual PV modules are the most commonly employed in PV system applications as seen in Fig.1. These topologies Although these inverters are achieved low THD values in the output voltage and current but they still have more controlled switches which are used to generate the required 7 level voltages. Therefore, these inverters are developed in this research as seen in section 3. Another advantage was presented in the proposed work, which is the simple unipolar phase disposition PD PWM modulation method that used instead of complex bipolar PWM technique [29,30].

SYSTEM DETAILED MODELING

Proposed RSMLI Structure

Figure 1 illustrated the proposed 7 levels RSMLI structure. In this structure, only seven switches and three diodes are used to obtain 7-levels at the output. The three individual PV arrays as DC voltage sources , along with three boost converters as the input each of $200V$ for achieving the required levels of output voltage across the inductive load. The boost converters are controlled by adjusting their duty ratio using FLMPPT technique. The proposed topology consists of seven MOSFET switches (SW_1, $SW_2, SW_3, SW_4, T_1, T_2$ and T_3) to produce 7 levels in one cycle, so the waveform of the output voltage will become nearly sinusoidal shape and then the THD content was decreased to well value. Besides MOSFETs, three diodes (D_1, D_2, D_3) are included in the main configuration to solve the issues of the bidirectional flow of the current.

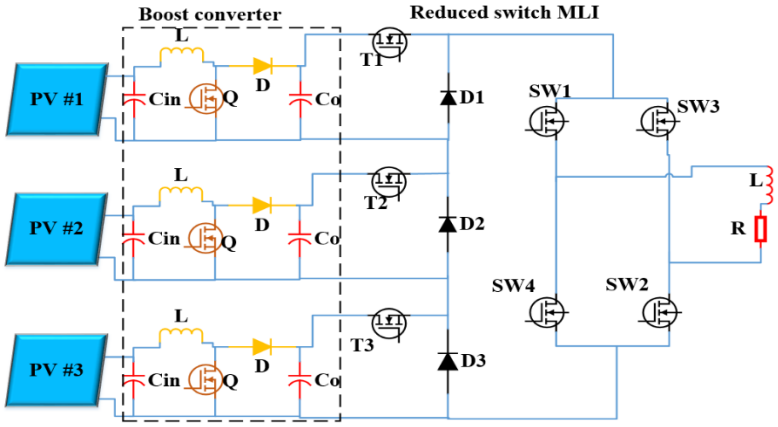


FIGURE 1. configuration of the proposed RSMLI topology.

Phase Disposition PWM Control

In order to obtain 7-levels at output, Fig. 2 should be investigated for one completed cycle. The angles distribution for the 7-level are divided between the switches that generate the levels which are conducted for completed time interval of ($20msec$). As seen, the angles for each switch of 7-level inverter were done between 0 to π for positive half cycle and switches conduction will repeated from π to 2π at the negative half cycle. The three MOSFETs named by (T_1, T_2, T_3) with helping the diodes are triggered by high switching frequency of ($5kHz$)to generate the levels while the H-bridge switches (SW_1, SW_2, SW_3, SW_4) are triggered with low frequency (50Hz) to produce the output polarity.

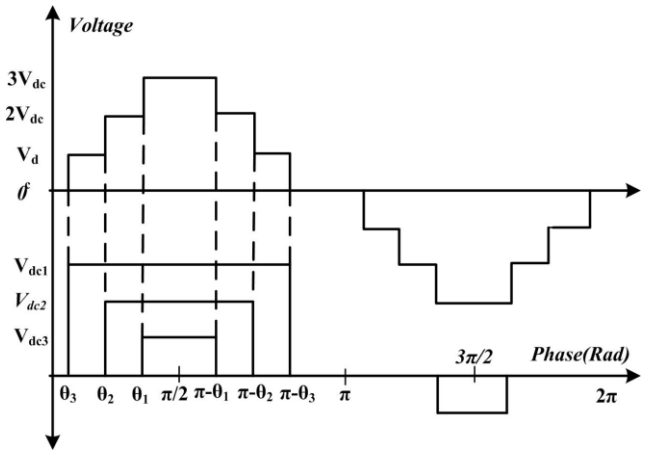


FIGURE 2. Angle distribution of one cycle for 7-level inverter.

The operation of the switching sequence for the 7-level proposed inverter is reported in Table1. As seen in Table 1, switches SW_1 and SW_2 are conduct through the positive half cycle to achieve the positive half at the output while switches SW_1 and SW_2 are conduct during the negative half cycle to obtain the negative half at the output. On other the hand, the levels switches are conduct according to the carriers PD PWM signals that compared with the reference sinewave signal. Unlike the high cost traditional PWM control methods used in [26-30], in this research the level switches are controlled by a simple unipolar PD PWM modulation technique. For this reason, the additional logical operators are avoided in this study. Therefore, the complexity, size and cost of the control circuit is reduced, and then the overall efficiency of the RSMLI is improved.

TABLE1. Switching sequence of proposed 7-level RSMLI circuit for one cycle.

OUTPUT LEVEL	SW_1	SW_2	SW_3	SW_4	T_1	T_2	T_3
$\mathbf{0V}$	1	1	0	0	0	0	0
$+\boldsymbol{V_{dc}}$	1	1	0	0	1	0	0
$+\mathbf{2}\boldsymbol{V_{dc}}$	1	1	0	0	1	1	0
$+\mathbf{3}\boldsymbol{V_{dc}}$	1	1	0	0	1	1	1
$+\mathbf{3}\boldsymbol{V_{dc}}$	1	1	0	0	1	1	1
$+\mathbf{2}\boldsymbol{V_{dc}}$	1	1	0	0	1	1	0
$+\boldsymbol{V_{dc}}$	1	1	0	0	1	0	0
$\mathbf{0V}$	1	1	0	0	0	0	0
$\mathbf{0V}$	0	0	1	1	0	0	0
$-\boldsymbol{V_{dc}}$	0	0	1	1	1	0	0
$-\mathbf{2}\boldsymbol{V_{dc}}$	0	0	1	1	1	1	0
$-\mathbf{3}\boldsymbol{V_{dc}}$	0	0	1	1	1	1	1
$-\mathbf{3}\boldsymbol{V_{dc}}$	0	0	1	1	1	1	1
$-\mathbf{2}\boldsymbol{V_{dc}}$	0	0	1	1	1	1	0
$-\boldsymbol{V_{dc}}$	0	0	1	1	1	0	0
$\mathbf{0V}$	0	0	1	1	0	0	0

Furthermore, SW_1 and SW_2 switch sequences are controlled by compare the reference sinusoidal signal with zero and then they are matching with the pulses. While SW_3 and SW_4 are matched with inverted these pulses. In this work, the levels switches are triggered by compare the absolute sinusoidal wave with the $P_1, P_2,$ and P_3 as seen in Fig.3. Time interval of the PWM signals is $[0\ 0.5\ 1]/5000$, where 5000 is the switching frequency used in this work. The output values of the carrier signals respect to the time interval are select as for $[0\ 1\ 0], [1\ 2\ 1], [2\ 3\ 2\ ]$ for $P_1, P_2,$ and P_3, respectively. The proposed control scheme is reported in Fig. 4

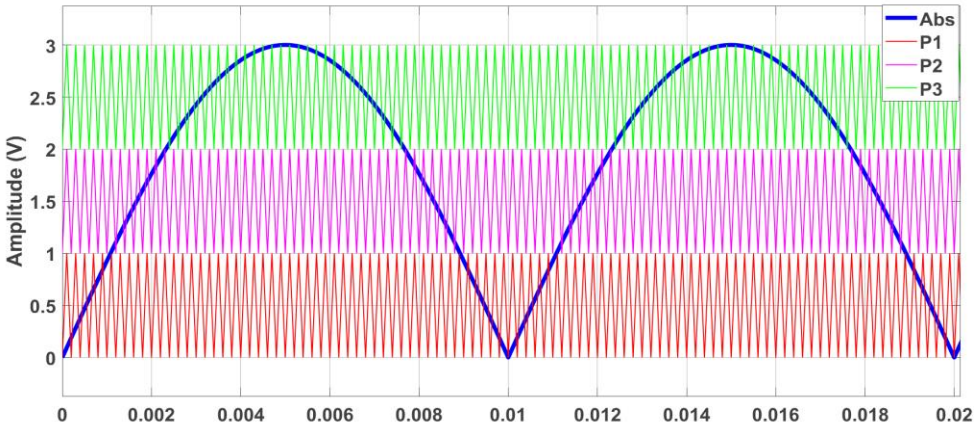


FIGURE 3. Unipolar PD PWM control scheme of proposed inverter.

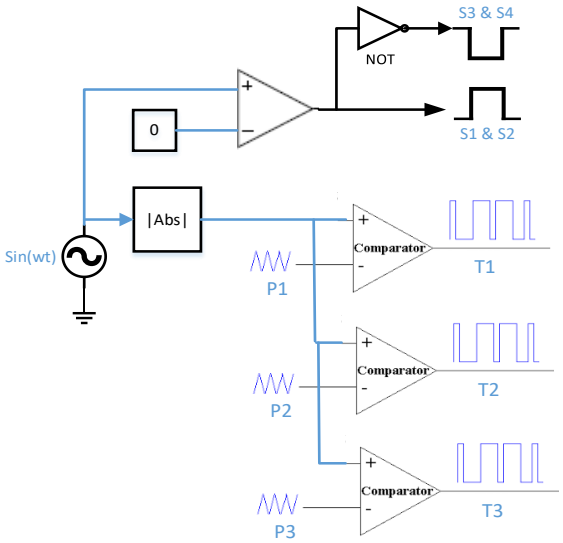


FIGURE 4. switching gate pulses of the proposed RSMLI topology.

Modeling of PV Array

In order to represent the mathematical model of a PV array, the single-diode PV model was used [4,5,8]. This model can be seen in Fig.5 which consists of photocurrent source, diode current, and shunt current branches. It is simple and easy to mode in any software and it provides sufficient representation for the PV module. However, the main equation of the output current (I)for a PV array for given $N_{ser} \times N_{par}$ can be written as follows [32],

$$I = N_{par}\, I_{pv} - N_{par}\, I_o \left[exp\left(\frac{V + R_s \left(\frac{N_{ser}}{N_{par}}\right).I}{\alpha\, V_{th} N_{ser}} \right) - 1 \right] - \frac{V + R_s \left(\frac{N_{ser}}{N_{par}}\right).I}{R_p \left(\frac{N_{ser}}{N_{par}}\right)} \quad (1)$$

Where I_{pv} is the photocurrent source, I_o is the saturation diode current, V is the output voltage of array, R_s is the series resistance, R_p is the parallel resistance, N_{ser} is the number of panels in series, N_{ser} is the no. of panels in parallel , α is the diode ideality constant, V_{th} is the thermal voltage $V_{th} = N_s KT/q.$, N_s is the number of cells in a PV panel, T is the temperature, K is constant of Boltzmann $(1.3806503\times10^{-23}\, J/°K)$, q is the charge value of electron $(1.60217646 \times 10^{-19} C)$.

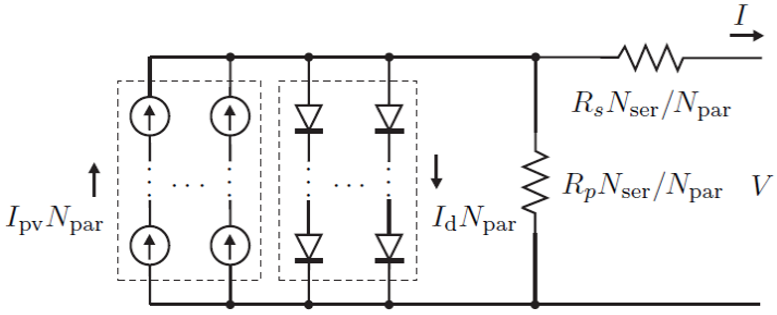


FIGURE 5. single-diode PV array circuit.

The photocurrent source can be written as follows [2,4]

$$I_{pv} = \left(I_{phn} + K_i \Delta T\right) \frac{G}{G_n} \quad (2)$$

Where $\Delta T = T - T_n$ ($T_n = 25°C$), G is the irradiance in W/m² while G_n is the reference value of irradiance which equals (1000W/m²) at STC, and K_i is the short-circuit temperature coefficient. The saturation current of diode can be computed as follows

$$I_o = I_{on}\left(\frac{T_n}{T}\right)^3 exp\left[\frac{qE_g}{\alpha K}\left(\frac{1}{T_n}-\frac{1}{T}\right)\right] \quad (3)$$

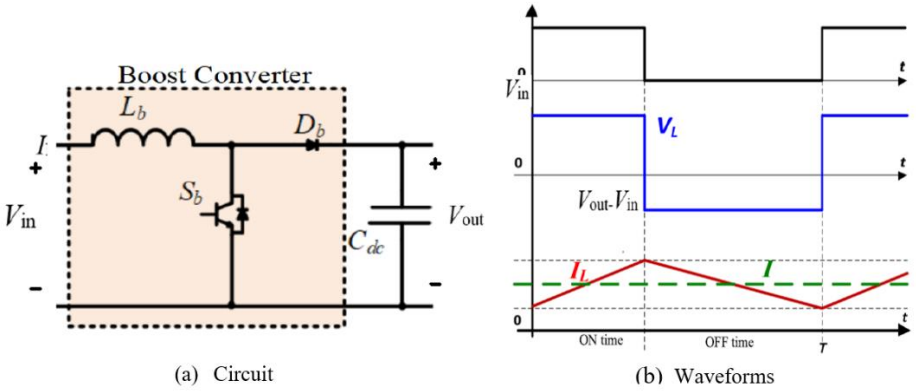
Where E_g is the bandgap energy. However, in this research, three individual PV arrays each array formed from 2×4 panels, so result a large PV array $P_{max} = 1600W$ to provide the suitable DC power and voltage to the RSMLI circuit. Besides, each PV array was integrated with DC/DC boost converter to raise the output voltage and implement the MPPT controller under different values of irradiance. Table 2 shows the electrical parameters of the used PV module under STC conditions.

TABLE 2. Parameters KC200GT solar PV panel at STC conditions.

Parameter	Value
Maximum power, P_{mpp}	$200W$
Open-circuit voltage, V_{oc}	$32.9\,V$
Maximum voltage, V_{mpp}	$26.3\,V$
Short-circuit current, I_{sc}	$8.21\,A$
Maximum current, I_{mpp}	$7.61\,A$
Current coefficient, K_i	$0.0032\,A/K$
Voltage coefficient, K_v	$-0.123V/K$
Number of cells, N_s	54
Shunt resistance, R_{sh}	$415.405\,\Omega$
Series resistance, R_s	$0.221\,\Omega$
Ideality factor, α	1.3

Boost Converter Modeling

The objective of using a MPPT controller is to increase the efficiency and improve the performance of the PV array[8,9]. In order to find the MPP, the matching between the PV module and the load depends on the load impedance must be satisfied. However, the step-up boost converter is most DC/DC converter used to implement a MPPT controller due to it has more advantages compared with other technologies. Besides, the boost converter can provide a higher output voltage at the load side, simple electrical structure, easy to implementation [9]. Figure 6 shows the electrical circuit and key switch waveforms of the boost converter.



(a) Circuit (b) Waveforms

FIGURE 6. Boost converter circuit (a) circuit wiring (b) key waveforms.

The output voltage and current of boost converter can be calculated from the following equation [8,9],

$$V_O = \frac{1}{1-d}V_{in} \quad (4)$$

$$I_O = I_L\ (1-d\ ) \quad (5)$$

The input inductor can be determined from Eq. (10) [8],

$$L = \frac{V_{in}\, d}{f_s\ \Delta I_L} \tag{6}$$

where f_s is the switching frequency, and $\Delta \mathrm{I_L} = 0.3\mathrm{I_L}$. Also, the value of the output capacitor can be calculated as in equation below:

$$C_O = \frac{I_O\, d}{f_s\ \Delta V_O} \tag{7}$$

where $\Delta \mathrm{V_O} = 0.02\mathrm{V_O}$. the input capacitor can be computed from [8] as below

$$C_{in} \geq \frac{d}{8 \times {f_s}^2 \times L \times 0.01} \tag{8}$$

Table 2 shows the design parameters of the boost converter under continuous conduction mode operation conditions.

TABLE 3. Electrical parameters of boost circuit.

Item	Value
L	0.1 mH
C_{out}	3000 μF
f_s	5000 Hz
C_{in}	3000 μF
d_{max}	0.8

SIMULATION RESULTS AND DISCUSSION

To validate the proposed RSMLI topology, MATLAB/simulink was used. The PD PWM modulation technque was done to obtaine the correcnt PWM pulses for the all swicths to obatin the 7-level output volatge as seen in Fig.7. it is clear that, the sequensc pulses of the switches are extracted during completed one cycle of 20ms.

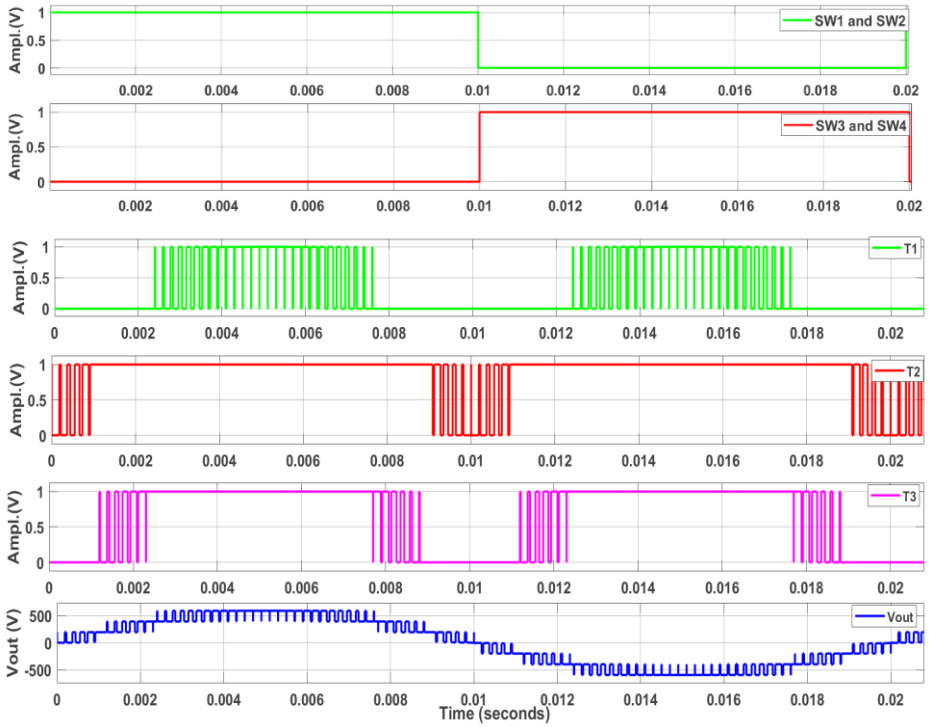


FIGURE 7. Proposed switching sequent waveforms for 7-level output voltage.

Furthermore, to test the performance of the proposed RSMLI applied on the standalone PV system many scenarios are done for simulation time $t = 1\,\text{sec}$ as following:

Scenario I: Performance at Constant Irradiance level

The proposed system was tested under constant irradiance level of $G = 1000W/m^2$ and constant temperature $T = 25℃$. The output voltage of each PV array with output voltage of the boost converters are shown in Fig. 8. As seen, each PV array has output voltage of $V_{PV} = 53V$, and this voltage was increased to $V_b = 200V$ which is represent the output voltage from each boost converter and then fed to the RSMLI circuit to build the required 7-level voltage at the output.

In this test, the proposed RSMLI was connected to pure resistive load of $R = 50\Omega$. Figure 9 reports the solar irradiance profile, DC voltage source of inverter, and the output voltage. The peak-peak output voltage equal from $600V$ to $-600V$, where this values are obtained during the 7 levels each level have DC voltage of $200V$.

Fig. 10 shows the voltage, current and power results of one PV array under constant environmental conditions. As seen, the steady state values for the voltage, current and power are of $53V$, $29A$ and $1600W$, respectively.

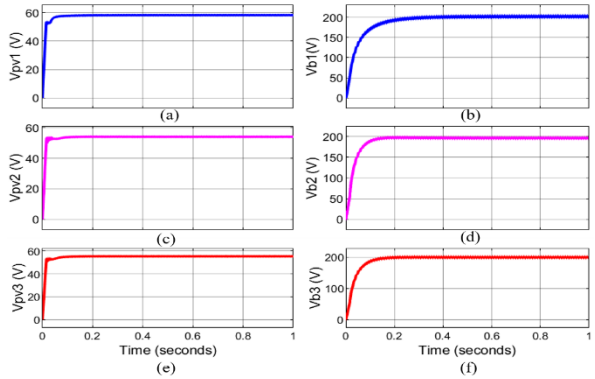


FIGURE 8. results of the PV and boost converters at constant weather conditions.

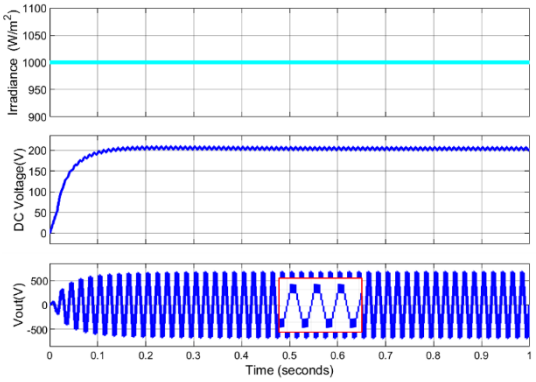


FIGURE 9. results of proposed RSMLI from top to bottom: irradiance, DC voltage of inverter, and output voltage

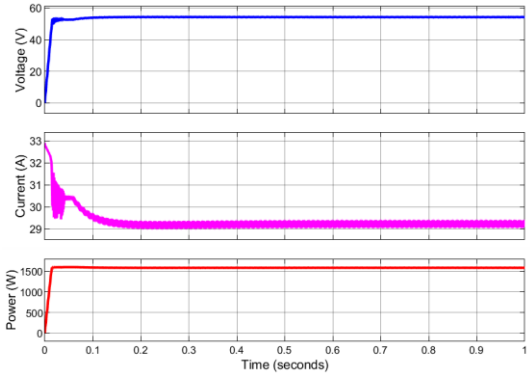


FIGURE 10. The voltage, current and power of one PV array under constant irradiance value.

Scenario II: Performance at a Step changes in Irradiance level

The irradiance level was varied at fast step as seen in Fig.11, from 1000 to 500 and then increased to 800W/m². it is clear that, the input DC voltage of inverter will decreased to 150V at solar irradiance of 500W/m² due to the reduction in the PV array voltage which affected by the irradiance levels. Also, the output voltage of the inverter decreased to 500V but it has the same 7-level at the output. Moreover, the reduction and increasing in irradiance effects strongly on the PV current and it effects slightly on the PV voltage, result decreasing in the maximum power of the PV array as seen in Fig. 12.

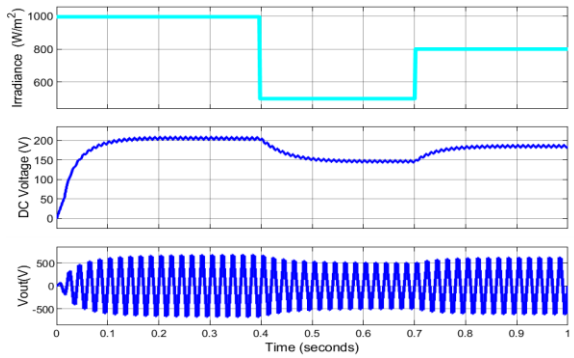


FIGURE 11. simulation results of proposed RSMLI from top to bottom at different values of irradiance: irradiance, DC voltage of inverter, and output voltage.

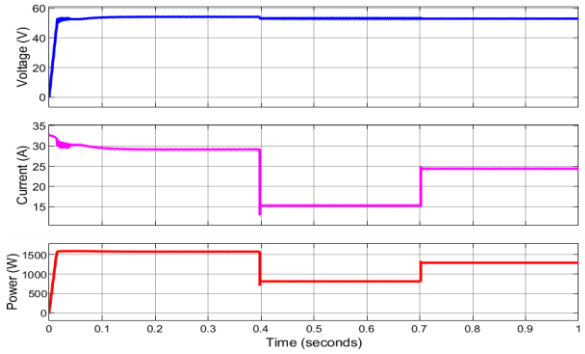


FIGURE 12. voltage, current and power of one PV array under varied irradiance level.

Scenario III: Test Performance at Different Load Conditions

In this section, the proposed RSMLI topology was tested under constant weather conditions and different load conditions to show the waveforms of the output voltage and compute the THD content in its waveform. First, the proposed inverter was connected throughout a pure resistive load of $R = 50\Omega$. Fig. 13 presents the simulation results of the output voltage and output current at resistive load conditions. As presented, both current and voltage at same phase and they have 7-levels. The value of the steady state value of the output voltage and current are 600V, and 12A, respectively. These values are obtained without filter where the THD content in the output voltage and current is low.

Fig. 14 illustrated the fast Fourier transform (FFT) analysis of the proposed inverter topology. As presented in this figure , $THD = 18.17\%$ was obtained without adding filter at resistive load side. The THD content in the output voltage and current is achieved according to the institute of Electrical and Electronics Engineers (IEEE) 519 harmonic distortion standard without filter which is allowable $15 - 25\%$. As a result, the proposed RSMLI provides good THD values compared to the values obtained in the conventional MLI topologies.

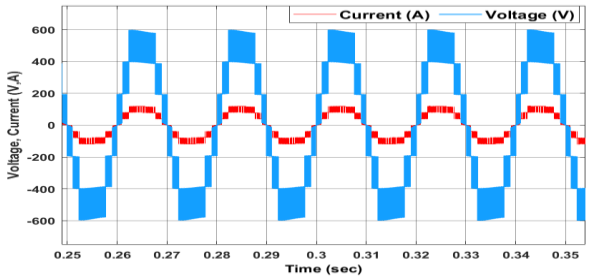


FIGURE 13. output voltage and current of proposed inverter without filter.

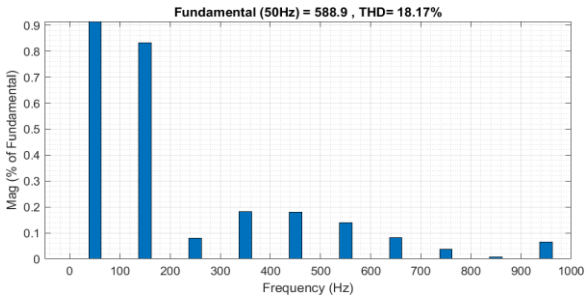


FIGURE 14. FFT analysis of proposed 7-level RSMLI with seven switches topology.

Figure 15 shows the output voltage and current of proposed inverter with L-C filter $L = 10mH$ and $C = 10\mu F$. The proposed 7-level inverter presented lower THD values which is $THD = 1.98\%$ which is in limits of IEEE institute ($\leq 5\%$) of THD with filter as seen in Fig.16.

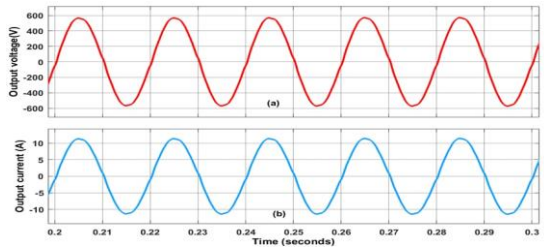


FIGURE 15. output voltage and current of proposed inverter with L-C filter.

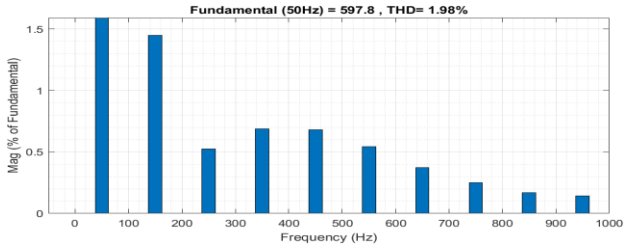


FIGURE 16. FFT analysis of proposed 7-level RSMLI with L-C filter.

Second, the proposed inverter was connected throughout inductive load of $R = 50\Omega$ and $L = 3mH$. The simulation results of the output voltage with current as seen in Fig. 17. Figure 18 illustrated the fast Fourier transform (FFT) analysis of the output voltage. As presented in this figure, $THD = 18.66\%$ was obtained without L-C filter. Fig.19 shows the output voltage and current of proposed inverter with L-C filter under inductive load conditions. %. the FFT analysis of the filtered output voltage was obtained as seen in Fig.20, where the proposed RSMLI inverter shows good agreement in terms of THD of 1.75%.

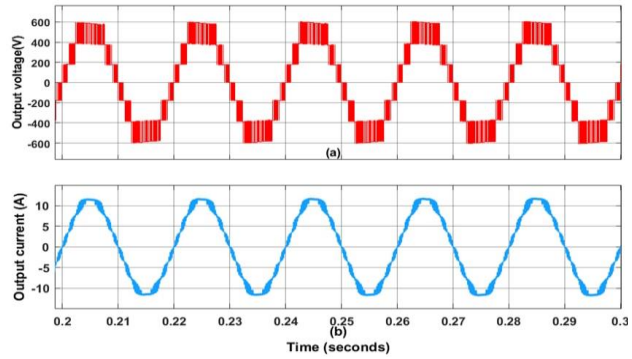


FIGURE 17. output voltage and current of proposed inverter at inductive load $R = 50\Omega$ and $L = 3mH$.

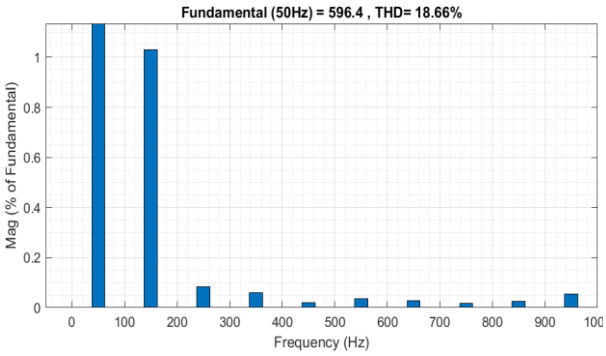


FIGURE 18. FFT analysis of proposed 7-level RSMLI without filter at inductive load.

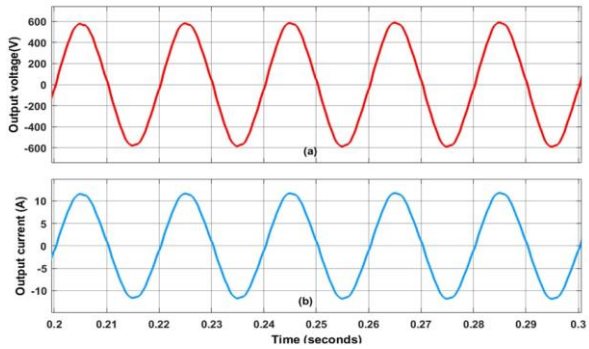


FIGURE 19. output voltage and current of proposed inverter with L-C filter at inductive load.

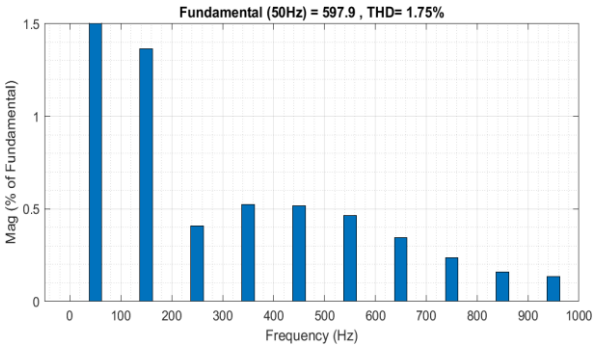


FIGURE 20. FFT analysis of proposed 7-level RSMLI with L-C filter at inductive load $R = 50\Omega$ and $L = 3mH$.

In summary, from the presented results it is clear that the proposed RSMLI with seven switches topology show good performance under different both weather and load conditions. In order to clear the main contribution of this work, Fig. 21 was presented. This figure shows the comparison of part count between the proposed RSMLI and other topologies available in the literature. As seen, the proposed inverter offers reduced no. of controlled switches, fewer no. of gate drivers and less no. of DC sources.

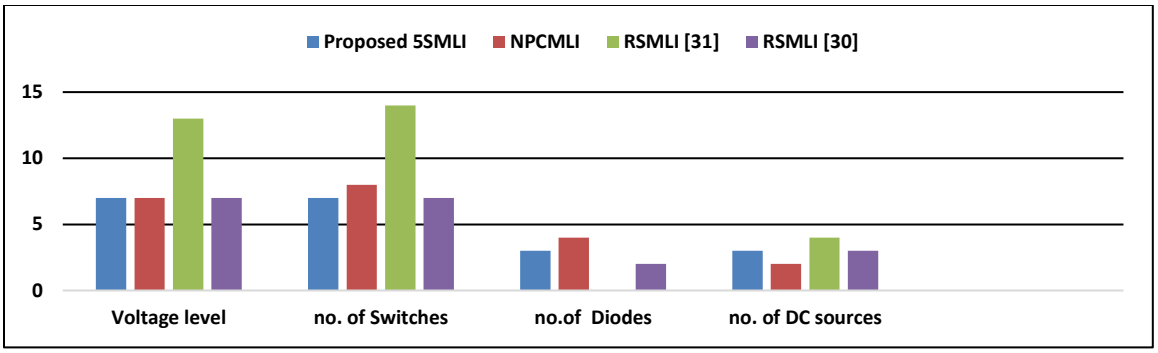


FIGURE 21. comparison of part components between the proposed 5SMLI and other topologies

CONCLUSION

In this paper, a reduced switch multilevel inverter (RSMLI) with seven switches was presented. the proposed MLI was designed with minimum number of switches compared to the conventional MLI topologies where it provides 7-level output voltage with only seven controlled switches and three diodes. Moreover, the phase disposition (PD) PWM based a simple unipolar technique was used to control the RSMLI switches. Compared to the bipolar PWM technique, the used technique in this research considers simple, low cost, and easy to the implementation. The proposed RSMLI topology was applied on a standalone PV system using individual PV arrays with three boost converters. Furthermore, each PV array was controlled using fuzzy logic MPPT technique and this controller was improved the efficiency and performance of the PV array especially at varied irradiance level. MATLAB/Simulink was used to test the performance of the proposed inverter under different scenarios. The simulation results show that the proposed topology offers lower THD content for the output voltage at resistive and inductive load conditions. Accordingly, the proposed RSMLI is compared with the other MLI topologies in terms of number of switches, number of levels ..etc. Form the comparison, the proposed topology was show low controlled switches and fewer gate drivers, and good THD values. A Grid-connected PV system based a RSMLI can be applied as a future work for this paper in order to enhance the grid and improve the power quality of the grid system.

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