Design and Software Implementation of Multilevel Diode Clamped Converter

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Design and Software Implementation of Multilevel Diode Clamped Converter

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Abstract. The work presented in this paper concerned with the design and software synthesis of multilevel diode clamped converter. Two topologies of this type of converters have been considered and tested. The first topology was three-level diode clamped converter, while the second one was the five-level diode clamped converter. The major task of the proposed work is to feed a three-phase load with semi-pure (low distorted) sinewave three-phase voltages. Simulation results show that an approximately unity power factor, low harmonic distortion and balance of capacitors voltages are achieved. The work presented for three level and five level to verify the positive effect of increasing the level of converter. The digital simulation is performed using the MATLAB / Simulink software.

1. Introduction

Recently, multilevel converters have gained much interesting due to their notable reduction in distortion and stress of the applied voltage, low electromagnetic interference (EMI), and low switching losses [1], [2]. Multilevel converter produces a stepped waveforms approximative to the sine waveforms [3]. According to the topology of the converter, these waveforms are supplied either from individual DC sources or from one DC source supported by a series connected capacitors. Employing the multilevel converters allows to divide the high DC voltage level into a several smaller DC voltage levels. This approach leads to manipulates low rating switching devices. Increasing the levels of these converters provides more steps which leads to an elegant stair case of the output waveforms that approaching closely to the sinewave [4]. Consequently, multilevel converters exhibit a sophisticated choice for the high-power applications because of the ability for handling high volt – ampere ratings with a significant reduction in the switching losses (i.e. dv/dt and di/dt losses) [3].There are three common types of multilevel converter topologies have been considered in the literatures these are [4 -6]:

- Diode clamped multilevel converters (DCMC).
- Flying capacitors multilevel converter (FCMC).
- Hybrid Bridge Multilevel Converters (HBMC).

In this paper, the DCMC will be employed to supply three phase loads with AC voltage from DC source to ensure high power quality (low distorted AC voltage and near unity power factor).

2. Diode Clamped Converter

DCMC is the most generally considered multilevel converter. In this type of converter, the diode is utilized as a "clamping Device" to hold the DC level for producing appropriate steps at the output waveform. Thus, the major notion of this converter is to restricts the stress of the voltage applied to the power switches with the aid of the diodes [4] , [7]. A (n) level DCMC converter requires (n-1) capacitors, 2(n -1) power switches and (n -1) (n-2) clamped diodes. As the number of the voltage levels are increased, high quality power delivered to the load is obtained and the load voltage shape becomes closer to the sine waveform [7-9].

Two topologies of this type of converters have been considered and tested: three level and five level DCMC. Figure 1 shows a three-level DCMC, the circuit includes two capacitors, C_1, C_2. If the amplitude of the dc supply voltage is Vdc, then the voltage through each capacitor is Vdc/2. Therefore, each power switches voltage stress will be restricted to the level of Vdc/2 by means of clamping diodes.

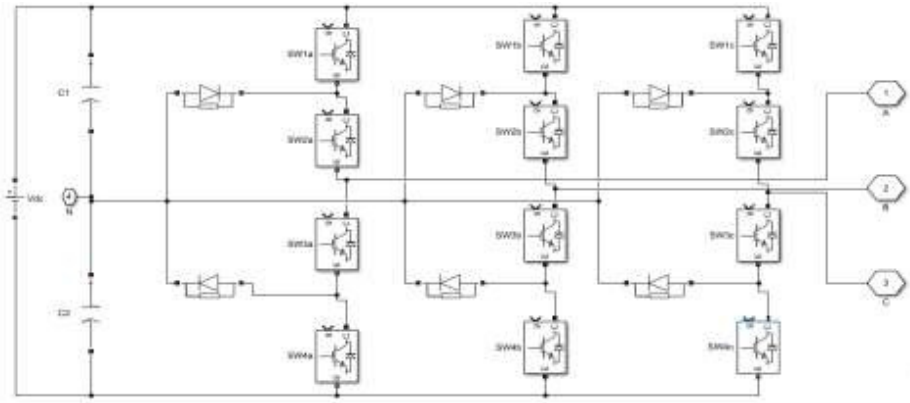


Figure 1. Structure of Three Level DCMC

Considering the operation of the three level DCMC per phase, the stepped voltage is synthesized according to table 1. The point N in Figure 1 is considered as the neutral of the output phase voltage [5],[10].

Table .1 Switching sequence for one phase Three level DCMC.

Sw1	Sw2	Sw3	Sw4	Voltage
1	1	1	0	+Vdc/2
1	0	0	1	0
0	1	1	1	-Vdc/2

From table 1, it's clear that there are three switch states that implement three-level voltages per phase. If phase A is considered, then the three levels of Van voltage are:

- Van= Vdc/2, when the switches Sw1a, SW2a and SW3a are in ON state.
- Van= 0, when the switches Sw1a and Sw4a are in ON state.
- Van= - Vdc/2 when the switches SW2a, SW3a and SW4a are in ON state.

The circuit that utilizes a three level DCMC for delivering three – phase AC voltage is shown in Figure 2.

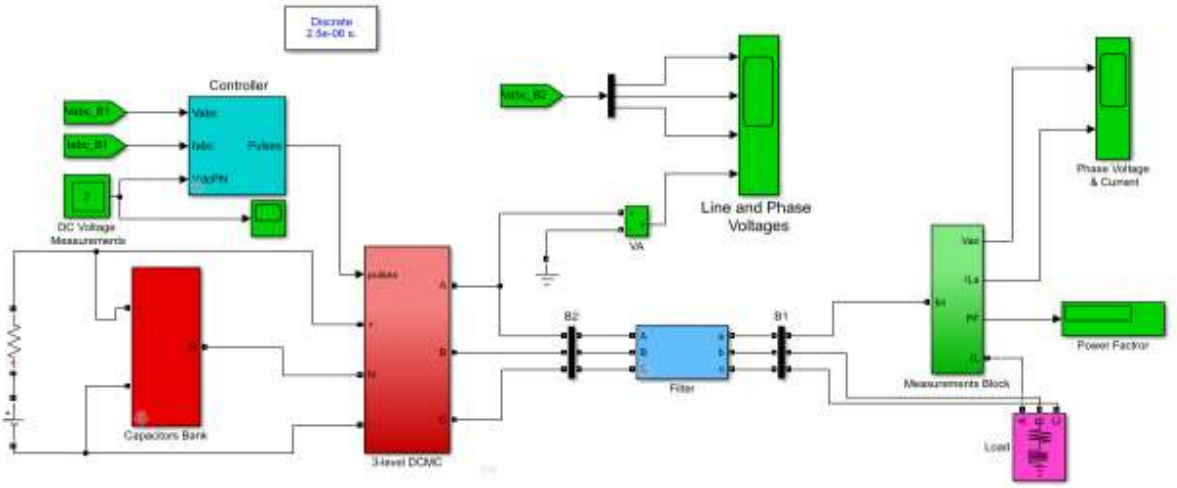


Figure 2. Three level DCMC simulation model

Figure 3 shows the five-level DCMC, the circuit contains of 4 capacitors, C_1, C_2, C_3 and C_4. If the magnitude of the dc supply voltage is Vdc, then the voltage through each capacitor is Vdc/4. Therefore, each power switch voltage stress will be restricted to the level of Vdc/4 by means of clamping diodes.

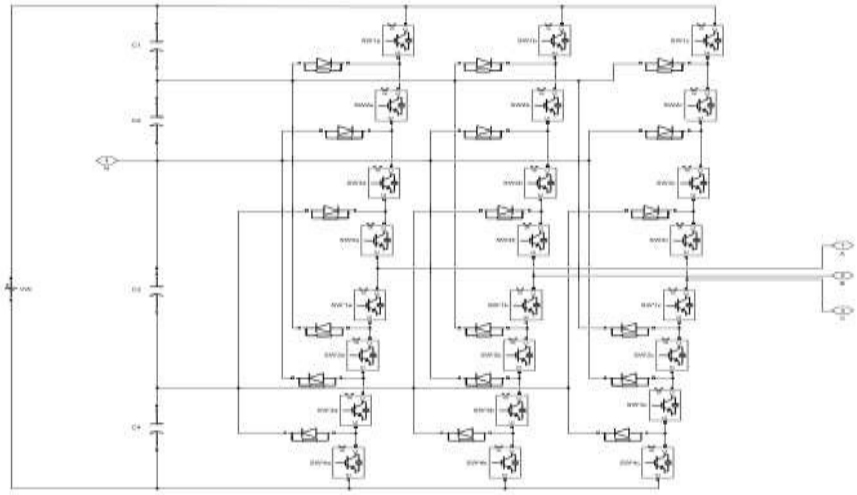


Figure 3. Structure of Five Level Diode Clamped Converter

Considering the operation of the three level DCMC per phase, the stepped voltage is synthesized according to table 2. The point N in Figure 3 is considered as the neutral of the output phase voltage [9-11].

Table .2 Switching scheme for Five level DCMC.

Sw1	Sw2	Sw3	Sw4	Sw1'	Sw2'	Sw3'	Sw4'	Voltage
0	0	1	1	1	1	0	0	0
0	1	1	1	1	0	0	0	+Vdc /4
1	1	1	1	0	0	0	0	+Vdc /2
0	0	0	1	1	1	1	0	-Vdc /4

0	0	0	0	1	1	1	1	-Vdc /2

From table 2, it's clear that there are five switch states that implement five-level voltages per phase. If phase A is considered, then the three levels of Van voltage are:

- Van= Vdc/2, the switches Sw1a, SW2a, SW3a and SW4a are in ON state.
- Van= Vdc/4, the switches Sw'1a, SW2a, SW3a and SW4a are in ON state.
- Van= 0, the switches Sw'1a, SW'2a, SW3a and Sw4a are in ON state.
- Van= -Vdc/4, the switches Sw'1a, SW'2a, SW'3a and SW4a are in ON state.
- Van= -Vdc/2, the switches Sw'1a, SW'2a, SW'3a and SW'4a are in ON state.

The circuit that utilizes a five level DCMC for delivering three – phase AC voltage is shown in Figure 4.

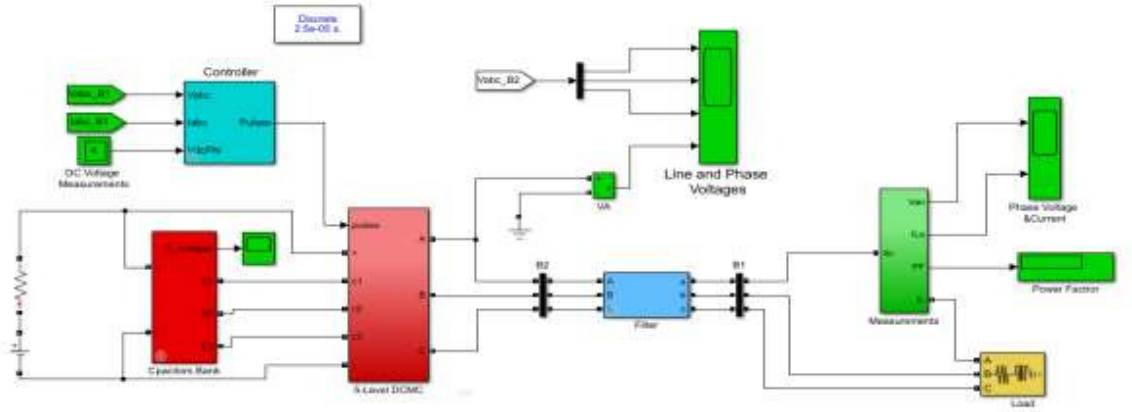


Figure 4. FLDCC simulation model

3. Control Strategy of the DCMC

The control algorithm of DCMC is implemented as shown in Figure 5 which performs the phase shifted PWM. According to the instantaneous values of the three phase voltages, the PLL block generate the angular frequency (ωt) as shown in Figure 6. This angular frequency is supplied to the measurement system block and firing pulses generator block.

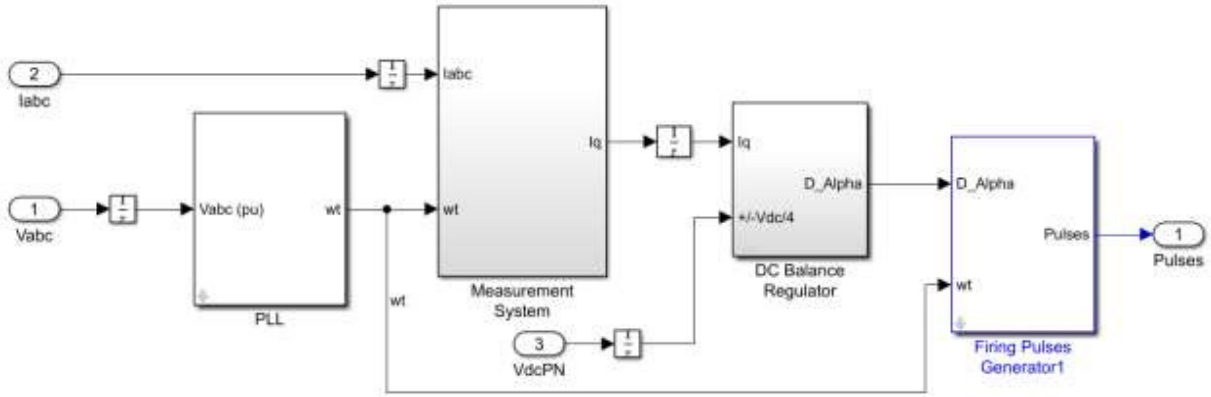


Figure 5. Control Bock Circuit for DCMC

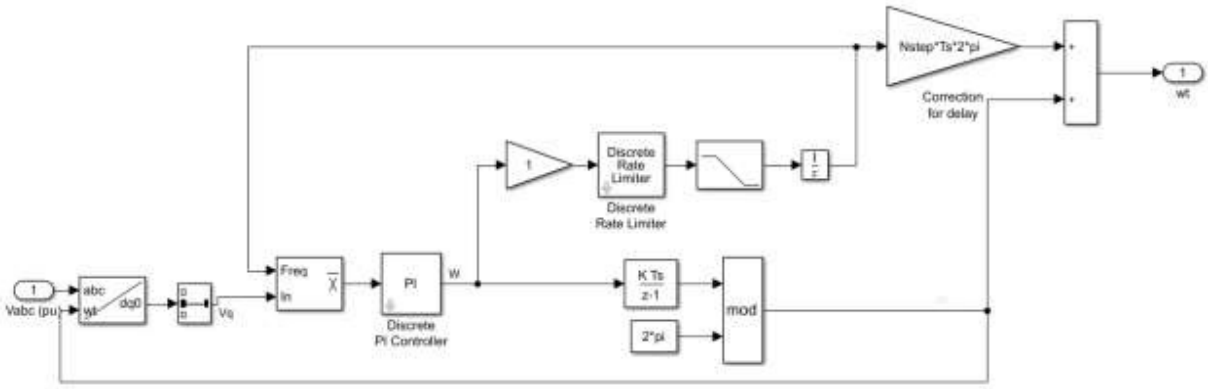


Figure 6. PLL circuit

The measurement system block generates the reactive current iq from the acquired data about the three – phase currents and the angular frequency (ωt) according to the following equation:

$$i_q = \frac{2}{3}(i_a cos\omega t + i_b \cos\left(\omega t - \frac{2\pi}{3}\right) + i_c \cos(\omega t + \frac{2\pi}{3}) \quad (1)$$

The calculated reactive current (iq) is employed in the DC balance regulator together with DC voltages across capacitors to produce the required modulating index D_{alpha}. The main block in this controller is the firing pulses controller block. For n level converter, this block is produces (n -1) waveforms as a carrier. These carrier waveforms will be compared with the reference sinusoidal waveform which has angular frequency of (ωt). The general operating principle of this block is as follows:

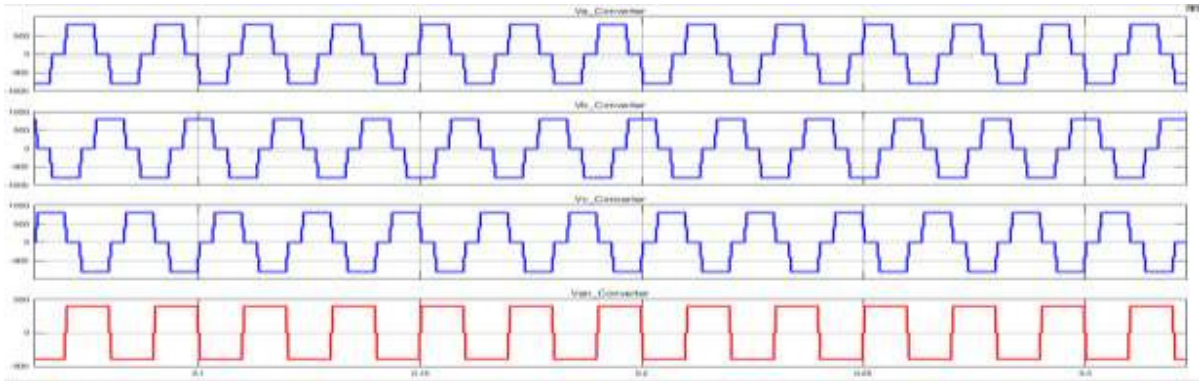
- If the reference signal is greater than all carrier signals, the converter switched to the full DC voltage.
- When the reference signal is less than the upper most carrier waveform, the converter switched to the half DC voltage.
- When the reference signal is less than lower most carrier waveform, the converter switched to the 0 V.

4. Simulation Results

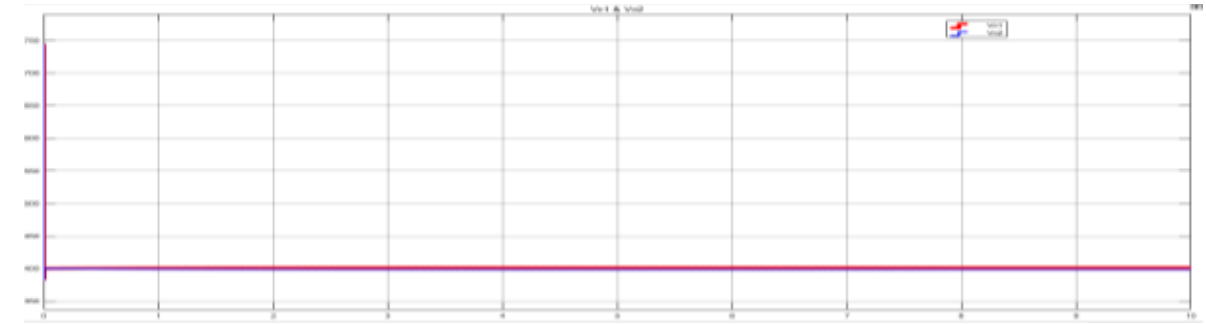
The simulation is carried out by MATLAB/SIMULINK software. The system parameters taken into account for the purpose of simulation are listed in Table 3. Figure 7 shows the simulation results of the three level DCMC, while Figure 8 shows the simulation results of the five level DCMC. The same load of 30 Kw and 10 Kvar was considered for both cases.

Table 3. System Parameters.

CONVERTER TYPE	NO. of switches per each arm	Dc Capacitor	DC-Link voltage	Phase voltage frequency	Phase voltage peak value'	Filter inductor	Filter capacitor	Three phase loads
TLDCC	4	400 mF	800	50	403	20e-3	850 µF	30kw,10Kvar
FLDCC	8	500 mF	800	50	403.8	19e-3	1000 µF	30kw,10Kvar



(a)



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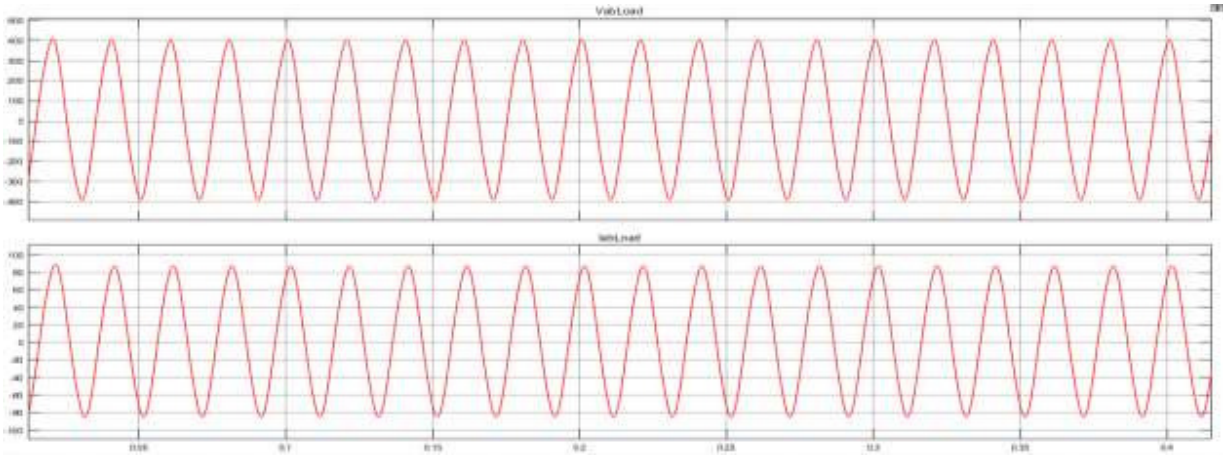

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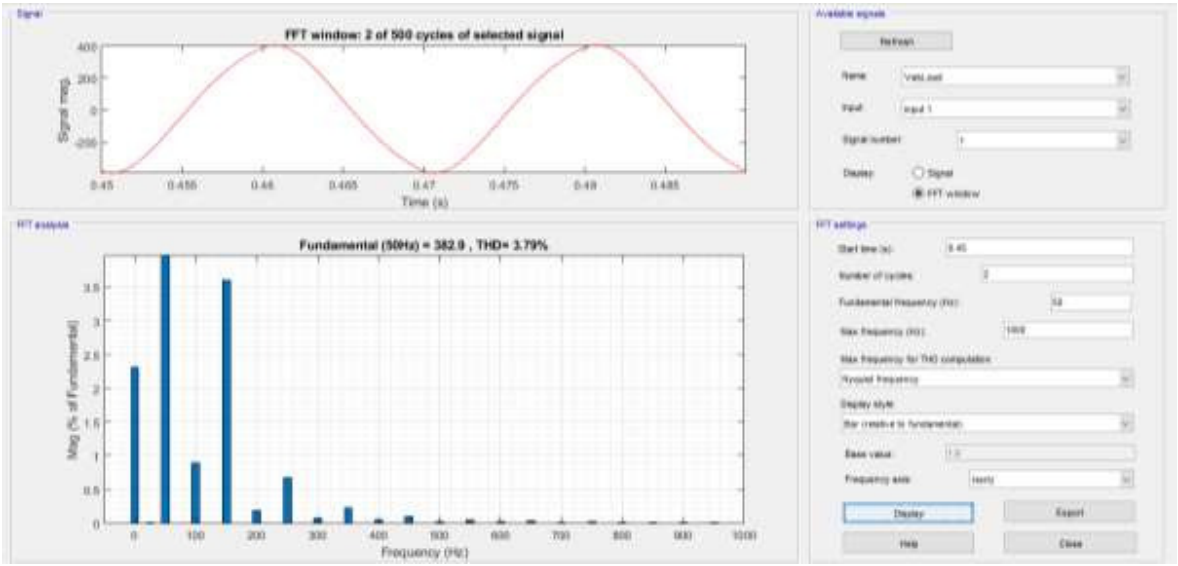
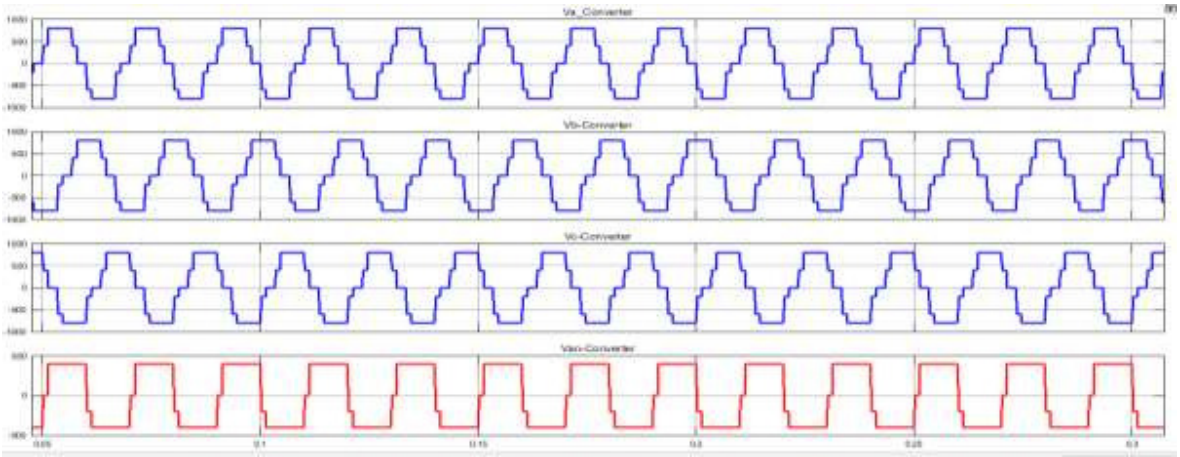
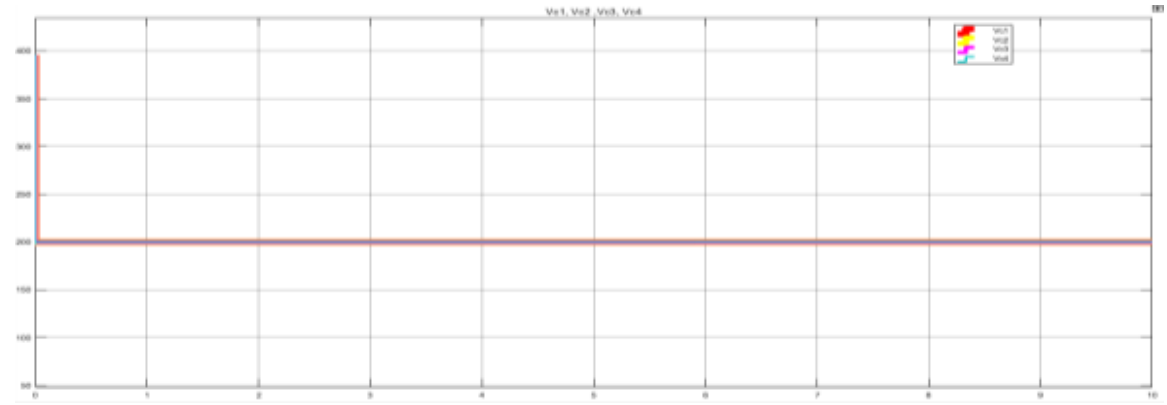


(d)

Figure 7. Simulation results for TLDCC (a) Line and Phase Voltages Waveforms (b) DC Link Capacitor Voltages Waveforms (c) Load Voltage & Load Current Waveforms (d) THD**.**



(a)



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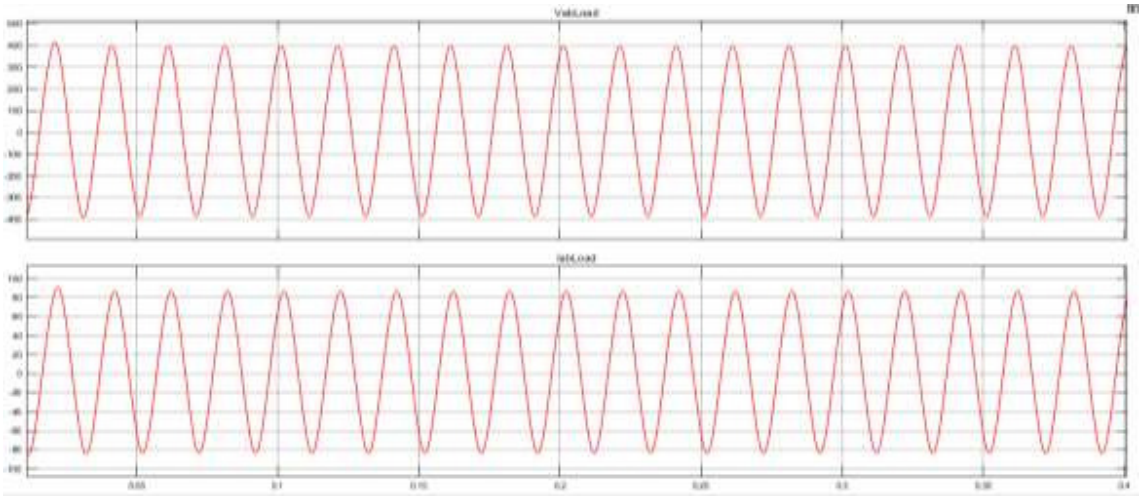

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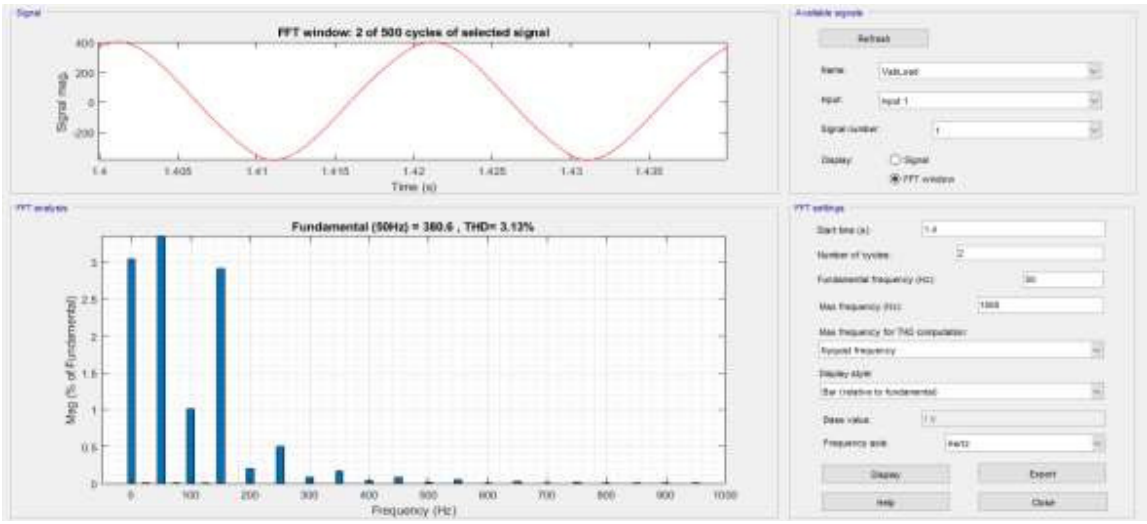

(d)

Figure 8. Simulation results for TLDCC (a)line and phase voltages waveforms (b)dc link capacitor voltages waveforms at no-load (c) Load voltage load current waveforms(d) THD**.**

Tables 4, 5 and 6 show the simulation results for the operation of three level DCMC, and the simulation results for the operation of five level DCMC with different loads. It is clear from the results shown that the requirements for high quality and low distortion of the power system for different load demands have been achieved.

Table 4. Simulation results for various loads.

Load Type	TLDCMC			FLDCMC		
RL	Phase voltage peak value	Power factor	THD%	Phase voltage peak value	Power factor	THD%
20kw,6Kvar	556	0.9578	2.28	500	0.9578	2.34
25kw,8Kvar	471	0.9524	2.64	460	0.9524	2.7
30kw,10Kvar	403	0.9487	3.79	403.8	0.9487	3.13

Table 5. Simulation results for resistive and capacitive load.

Load Type	TLDCC			FLDCC		
RC	Phase voltage peak value	Power factor	THD%	Phase voltage peak value	Power factor	THD %
20kw,6Kvar	413	0.9578	2.62	361	0.9578	2.79
25kw,8Kvar	353	0.9524	3.03	330	0.9524	3.14
30kw,10Kvar	312	0.9486	3.47	295	0.9486	3.48

Table 6. Simulation results for resistive load.

Load Type	TLDCC			FLDCC		
R	Peak voltage value	Power factor	THD%	Peak voltage value	Power factor	THD%
20kw	488	1	3.07	423	1	2.46
25kw	420	1	3.48	373	1	2.76
30kw	388	1	3.91	338	1	3.06

5. Conclusions

This paper presents the design and software implementation for three level and five level of diode clamped converter. Phase shifted PWM control is employed to the considered converter. The designed converters provide low distorted sine wave to the load with high quality (near unity power factor). Simulation results obtained show that the higher-level converter (FLDCMC) provides good result for harmonic distortion compared with TLDCMC for the same load. Two types accomplished equal power factor at the same load.

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