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Simulink Implementation of Voltage Stability Improvements Using STATCOM based 5-level Diode Clamped Converter

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Abstract. In this paper, a STATCOM based on Five-level Diode Clamped Multilevel Converter is used to maintain the bus voltage at specific bus bar in a suggested grid under various abnormal conditions like 2-phase to ground fault, load disturbance and source disturbance. The suggested grid consists of a single machine, transmission line and loads. The compensation procedure is carried out and compared between the two suggested control methods, the first method was the traditional control method using Phase Shifted-PWM controller which is used to improve the voltage profile. The Second one was the Finite Set-Model Predictive Controller for improving the voltage profile. The simulation results show that the two methods provided significant improvements of the bus voltage profile. Moreover, the improvement of voltage profile using FS-MPC method is less over shoot and attains a steady state better than the conventional PS-PWM when the system is subjected under many disturbances. The results of the harmonic effect show low values of total harmonic distortion (THD) of supply voltage and current.
Keywords: diode clamped multilevel converter, STATCOM, Phase shift carrier Pulse width modulation, Finite set model predictive control

1.Inroduction.

Increasing power request, environmental condition, and traditional planning lead to voltage destabilization in power systems. Voltage instability is defined as an issue which results in a greater power outage. To enhance the power system and for more stable and efficient power system, flexible AC transmission system (FACTS) is utilized and connected at weak bus of the system. The FACTS technology is very important in order to mitigate certain problems, not all of them, by ensuring that the power utilities get the most out of the transmission facilities and boost grid reliability [1] [2]. Multilevel voltage source converter-based compensators are considered one of the most flexible and powerful FACTS controllers for efficiency improvement, power flow management and grid voltage regulation. Multilevel inverters have many advantages compared to conventional two-level VSI, as with reduced harmonic distortion, increased AC voltage, reduced voltage stress on power devices, operation with reduced switching frequency, and high reliability. Due to these features, multilevel inverters are now very important in medium and high-power applications. Multilevel inverter provides high voltage capability together with low distortion voltages favors them in FACTS. One of the FACTS equipment using multilevel converters is the STATCOM [3].

STATCOM contains a VSC (Voltage Source Converter), Dc capacitor and coupling transformer [4] . Its output current (inductive or capacitive) can be controlled independently of the AC system voltage. During steady-state, STATCOM maintain reference component of the VSC voltage in same phase with the grid voltage Vgrid. It generates capacitive reactive power Q if the VSC voltage greater than Vgrid and absorbs inductive reactive power Q if the VSC voltage less than Vgrid [5]. The quantity of Q is often limited consistent with the magnitude of VSC voltage and the transformer leakage reactance. Numerous topologies have been validated in STATCOMs, the most popular of which are the cascaded multilevel H-bridge converters [6], diode clamped multilevel converters [7], multilevel flying capacitor converters [8].

Mainly, using the DCMC ensures modification of the converter's output voltage and promotes working at voltage and power with higher-rate. In addition, increasing the voltage levels in the converter results in a substantial reduction in the line currents' total harmonics distortion (THD). In Diode Clamped Multilevel Converter (DCMC), the (m) level DCMC converter requires (m-1) capacitors, 2(m -1) power switches and (m -1) (m-2) clamped diodes. As the number of the voltage levels are increased, high quality power delivered to the load is obtained and the load voltage shape becomes closer to the sine waveform [9] [10]. One of the major research concerns in the 3-phase multi-level inverter is the control strategy issue, particularly for power quality enhancement applications, which require converters to guarantee fine voltage distortion reduction and increase power factor [11]. Several control techniques have been proposed for STATCOM control to enhance the stability of the voltage. These control techniques can classify into traditional and modern techniques. In this paper, the traditional control technique Phase Shifted-PWM and the modern technique Finite Set-Model Predictive Control will be applied at test grid in order to compare between the behavior of the techniques and illustrate their effect in improving voltage profile and enhance maximum stability limit.

2. PS-PWM Control Technique

The PS-PWM approach is based on creating the reference voltage using the traditional PWM technique applicable to each converter topology power cell. In addition, taking into account the interleaving principle, a phase shift is imposed between the power cells in order to reach the optimum quality of the output waveforms. The PS-PWM approach achieves efficient distribution of power between cells with the same dc voltage and the same reference voltage for each power cell [12]. The PS-PWM has (m-1) carriers with a frequency of:

$$\omega_{carreir'} = \frac{\omega_{carrier}}{m-1} \quad (1)$$

Where, $\omega_{carrier}$ is the switching frequency of producing PWM waveform [13]. In basic PS-PWM scheme, all the triangular carriers have the same peak-peak amplitude and same frequency. The carriers shifted from each other by a phase shift $\varphi_{carreir}$ as described in equation (2) below [14]:

$$\varphi_{carreir} = \frac{\pi}{m-1} \quad (2)$$

The modulating signal is a sinusoidal wave with adjustable frequency, phase angle and amplitude [15].

3. FS-MPC Control Technique

Finite set model predictive control (FS-MPC) strategy is based on the discrete mathematical model and restricted switching combinations. The key features of the method are that the problem of optimizing can be easily solved by calculating the limited switching combinations for the regulated variants in a predefined cost function equation within a finite time period, without the presence of a module of pulse width modulation (PWM) [16]. The behavior of the converter is predicted by the FS-MPC for the limited possible voltage vectors at each sampling interval. For this control strategy the cost function should be defined to estimate the voltage vector for the future sampling interval, the optimal switching time is picked out and implemented to the converter to minimize the cost function. The target of this control is minimizing error between reference value and predicted value for the current [17]. FS-MPC is usually implemented in αβ-frame [18]. FS-MPC generic control diagram is illustrated in Figure 1. The main element in the modeling of a converter is the power switch such as (IGBTs and GTOs). The ideal switch has only two states: 'ON' state and 'OFF' state. As each switch has different combinations of the two switching states, some of these

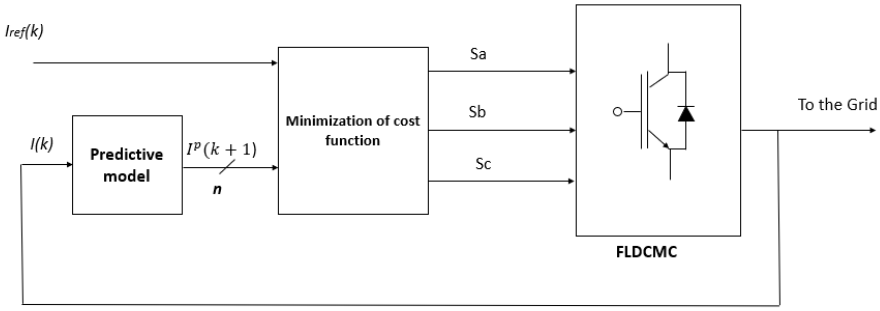


Figure 1. FS-MPC generic control diagram

combinations will short-circuit the DC link. Therefore, The total switching states of FLDCMC are 125 states (symbol *n* in Figure 1 represents these states) , while there are some states are redundant and produce the same voltage vector, therefore the converter can apply 61 different voltage vectors to the load from the total number of switching states [19]. The voltage vector for the output voltage can be represented as in equation (3):

$$v = \frac{2}{3}(v_{an} + av_{bn} + a^2 v_{cn}) \quad (3)$$

The symbol (a) is the complex operator $a = e^{\frac{j2\pi}{3}}$, v_a, v_b *and* v_c are the voltages obtained according to Table 1**.** The cost function to minimized by the FS-MPC is described in the following equation [17]:

$$g = \left|i_\alpha^*(k+1) - i_\alpha^p(k+1)\right| + \left|i_\beta^*(k+1) - i_\beta^p(k+1)\right| \quad (4)$$

Where i_α^* is the real component of reference current, $i_\beta^*$is the imaginary component of the reference current, $i_\alpha^p$is the real component of predicted current and $i_\beta^p$is the imaginary component of predicted current at the adjacent sampling interval (k+1). The reference current is created typically with an external controller (almost PI controller) that guarantees the required reactive power injection and the ultimate DC voltage regulation [18]. While, the load current at sample interval (k) is measured, then the model will estimate the value of load current for (k+1) at each voltage vectors, and the cost function find the error between reference predicted values, these steps lead to choose the voltage that will minimize the error. The load current expressed in discrete-time model by the following equation [20] [21]:

$$\frac{di}{dt} = \frac{i(k+1) - i(k)}{T_s} \quad (5)$$

And the prediction load current for (k+1) is expressed as:

$$i^p(k+1) = \left(1 - \frac{RT_s}{L}\right) i(k) + \frac{T_s}{L}\left(v(k) - e'(k)\right) \quad (6)$$

Where R and L is the resistance and inductance of the load, e' is e.m.f and it is represented as:

$$e'(k-1) = v(k-1) - \left(\frac{L}{T_s}\right) i(k) - \left(R - \frac{L}{T_s}\right)(i(k-1) \quad (7)$$

4. STATCOM Configuration

In this paper a design of a static synchronous compensator (STATCOM) based on diode clamped multilevel converter DCMC installed on the 11kV, 100MVA distribution system is considered. The exchanging process between the power system and the converter can be described by the following equation [22]:

$$Q = \frac{V_{conv}(V_{conv} - V_{bus})}{X_f} \quad (8)$$

STATCOM is designed and tested based on five-level diode-clamped converter (FLDCC) as shown in Figure 2.

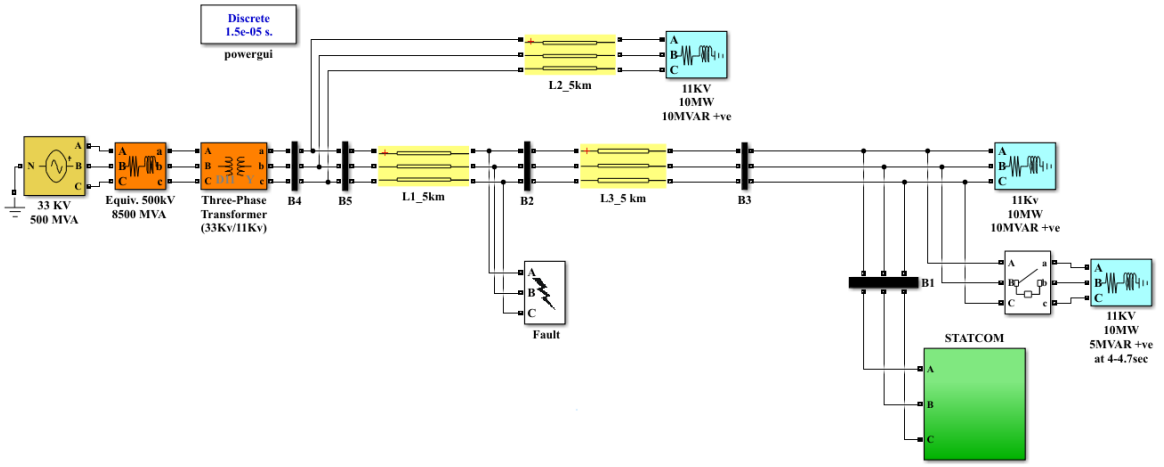


Figure 2. Power system with a STATCOM

STATCOM structure consists of 3-phase,5-level DCMC connected to the grid in series through 4 – zig – zag transformers. The 5-level DCMC structure is shown if Figure 3, which consists of 4 capacitors (C1, C2, C3 & C4), 24 IGBTs and 18 clamped diodes. The voltage per each capacitor is Vdc/4. Taking in the consideration the operation of 5-level-DCMC per phase, the stepped voltage formed as per Table (1). A point 'N' in Figure 3 represents the neutral of output phase voltage.

Table 1. Switching scheme for 5-level DCMC [23]

$Sw1_a$	$Sw2_a$	$Sw3_a$	$Sw4_a$	$Sw1_a$'	$Sw2_a$'	$Sw3_a$'	$Sw4_a$'	Voltage
0	0	1	1	1	1	0	0	0
0	1	1	1	1	0	0	0	+Vdc /4
1	1	1	1	0	0	0	0	+Vdc /2
0	0	0	1	1	1	1	0	-Vdc /4
0	0	0	0	1	1	1	1	-Vdc /2

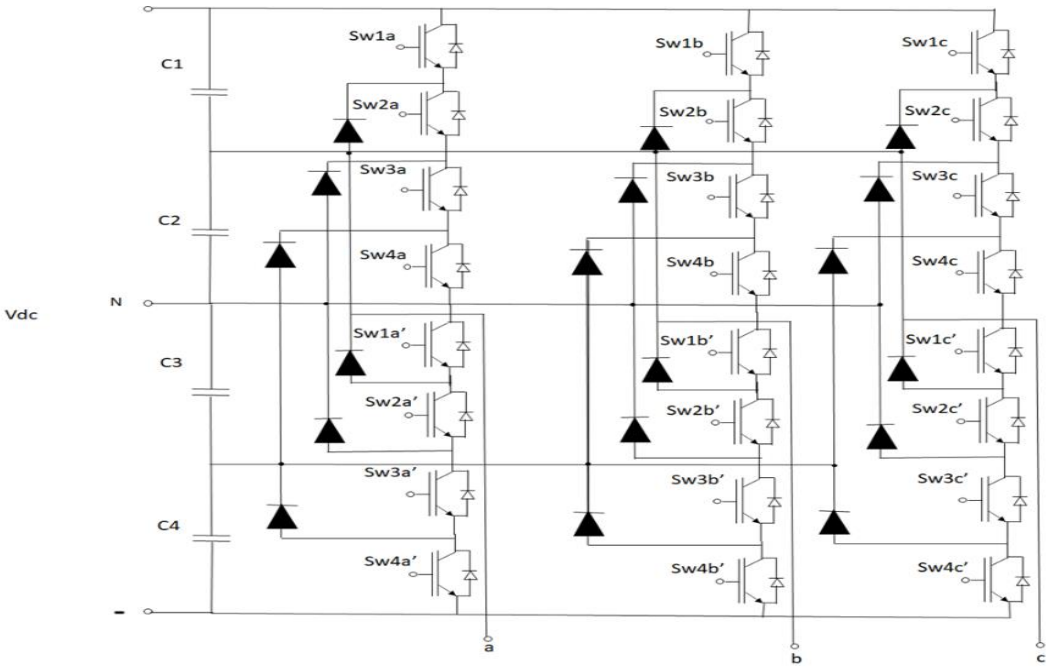


Figure 3. Structure of 5-level DCMC

5. STATCOM Controller

In order to enhance voltage regulation in the suggestd power system, the two techniques:PS-PWM and FS-MPC will be implemented. As the two techniques have different implementation in STATCOM controler, the main descrbtion of thier desingns will be illustated in this section.

5.1 STATCOM Controller based PS-PWM Technique

The STATCOM controller based PS-PWM Technique illustrated in Figure 4 consists of measurement system, phase locked loop PLL, voltage regulator, I_q limit computation and I_{qref} selection, current regultor, DC balance regutor and firin pulses.

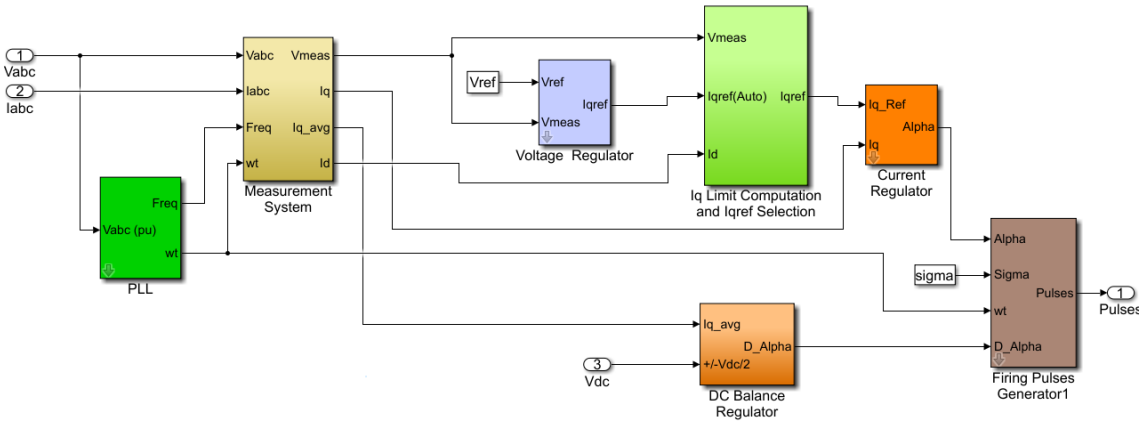


Figure 4. STATCOM controller

A phase locked loop (PLL) detects on the positive sequence component of the 3-phase V_{abc} of the measurement Bus 1. The components of the 3-phase ac system for the direct-quadrature axes evaluated by the output of the PLL (ωt), where V_q and V_d represent three-phase voltages, and I_d and I_q represent three-

phase currents. Measurement system measures direct axis and quadrature axis components of AC positive sequence voltage and currents to be controlled as well as the DC voltage V_{dc}. The AC voltage regulator is a proportional integral regulator (PI) compute the signal error between V_{ref} and actual voltage V_{ac} and supply I_{qref} "the quadrature reference current" for the current regulator. While the DC voltage regulator which is also PI regulator, supplies I_{qref} "the direct reference current" for the current regulator. The current regulator determines the magnitude and the phase of voltage produced by PWM converter from the reference currents (I_{dref} and I_{qref}) [24] [25]. The output signal of the PI controller Alpha (α) represents the required phase shift between the STATCOM voltage and the power system voltage. The required inputs for DC balance regulator are ($I_{q\text{-}avg}$) and DC link voltage. The dc voltage deviation is corrected by PI to obtain the desired modulating index D_{alpha} (or Δα) which is required to be used for charge / discharge capacitors to balance voltages across the two capacitor chunks which invalidate the error signal. The DC link voltage is represented as (Vdc/(*m*-1)), where *m* represents the number of capacitors according to the DCMC used. At firing pulses generator, alpha, D_{alpha}, ωt and Sigma (or σ: prevalent conduction angle) are applied at 3-phase bridges to produce (*m* -1) waveforms as a carrier for *m* level converter. These carrier waveforms will be compared with the reference sinusoidal waveform so as to generate the required firing pulses. Phase shifted carrier PWM technique required four carrier signals in FLDCC to allocate limits between voltage levels. In PSC-PWM the *m*-carriers signals have the same amplitude and frequency, but shifted each signal from the other by 45 degree in FLDCC where the number of carrier signals are four.

5.2 STATCOM using FS-MPC strategy

Figure 5 shows the FLDCMC configuration as a STATCOM using FS-MPC algorithm. The principle work of STATCOM using FS-MPC is the same as the principle work of STATCOM using PS-PWM except in the pulse generation method, where the cost function will be utilized for this purpose in STATCOM using FS-MPC. In the minimizing function block, the inputs are I_{ref} and I_{meas}, and the output is the pulses that fed to the FLDCMC. As illustrated in section 2, FLDCC can apply 61 unique voltage vectors from the total number of switching states, therefor, the cost function is evaluated for each of the 61 possible voltage vectors. The switching state associated with the voltage vector that minimizes the cost function is selected and applied during the next sampling instant.

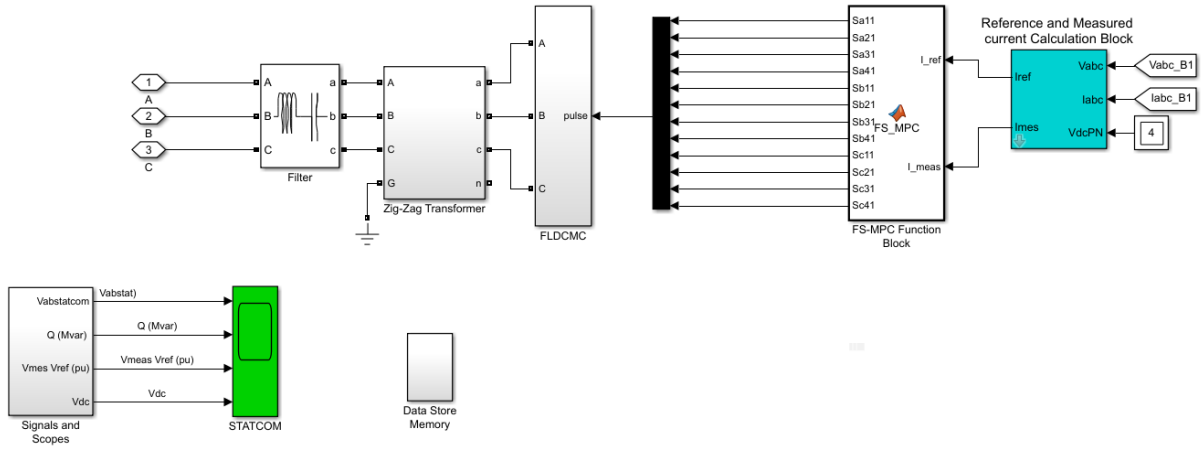


Figure 5. Model of STATCOM using FS-MPC strategy

5.3 Currents Calculation Block

The main task of Currents Calculation Block is to determine the reference and mesured currents (I_{ref} & I_{meas}) in αβ coordinate form which are supplied to the FS-MPC function block. The Currents Calculation Block includes: PLL, Measurement system,Voltage regultor. PLL and Measurement system in this controller have the same design of those used in PS-PWM controller. Voltage regultor consists of two PI controller as shown in Figure 7 to create I_{dref} and I_{qref}.

- **To produce I_{dref} ,** the resultant error signal from subtracting reference voltage value (V_{dc_ref}) and measured (V_{dc}) fed to PI controller. The error signal is subtracted from feedback signal of proportional-integral (PI) controller. The output signal of PI controller I_{ref} is represented by summation proportional and integral signals and limited by saturation limiter.

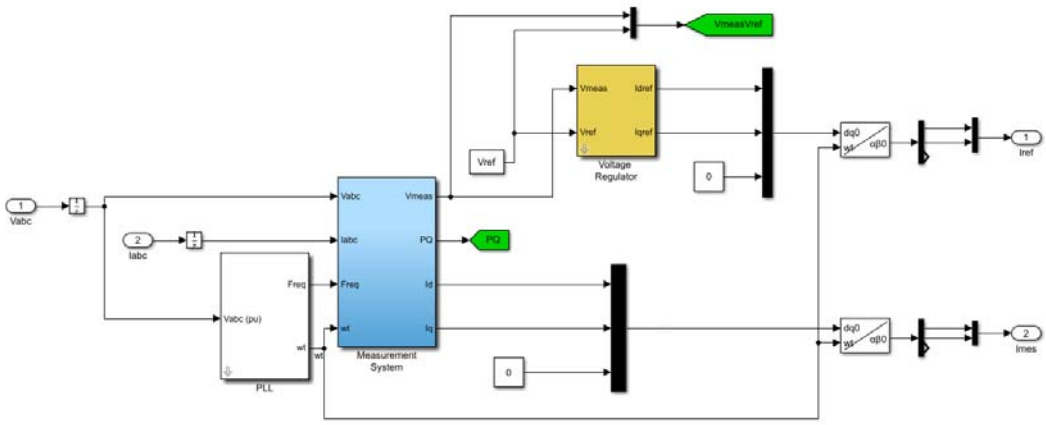


Figure 6. Controller of STATCOM using FS-MPC

- **To produce I_{qref} ,** the resultant error signal from subtracting reference voltage value (V_{ref}) and measured AC voltage (V_{meas}) fed to PI controller. The error signal is subtracted from feedback signal of proportional-integral (PI) controller. The output signal of PI controller I_{qref} is represented by summation proportional and integral signals and limited by saturation limiter.

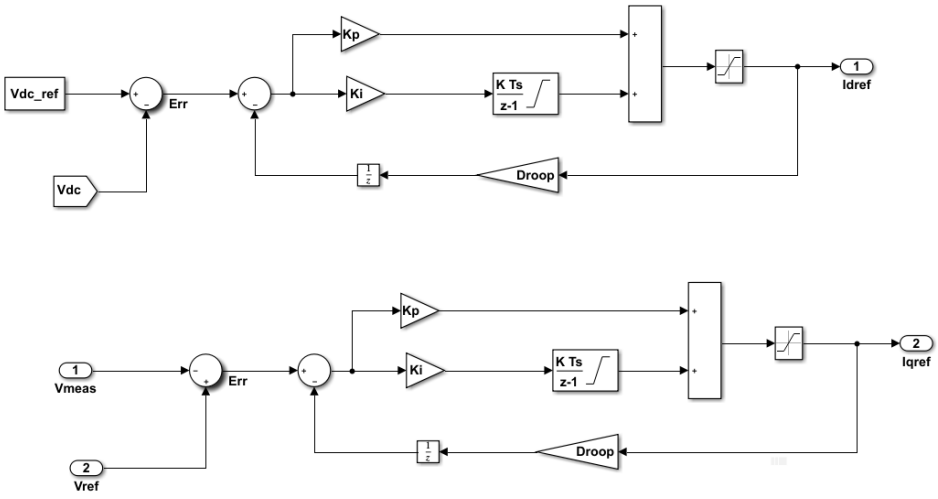


Figure 7. Voltage regulator STATCOM using FS-MPC strategy

1. **dq-αβ transformation units:** these units are utilized to compute I_{meas} and I_{ref} by using Inverse Park matrix which is represented as in the following equation:

$$\text{Inverse Park Matrix} = \begin{bmatrix} cos\omega t & -sin\omega t \\ sin\omega t & cos\omega t \end{bmatrix} \quad (9)$$

$\mathbf{I}_{meas}$ results from converting I_d and I_q to I_α and I_β as shown in the following equation:

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} cos\omega t & -sin\omega t \\ sin\omega t & cos\omega t \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \quad (10)$$

$\mathbf{I}_{ref}$ results from converting I_{dref} and I_{qref} to I_α and I_β as shown in the following equation:

$$\begin{bmatrix} I_{\alpha ref} \\ I_{\beta ref} \end{bmatrix} = \begin{bmatrix} cos\omega t & -sin\omega t \\ sin\omega t & cos\omega t \end{bmatrix} \begin{bmatrix} I_{dref} \\ I_{qref} \end{bmatrix} \quad (11)$$

6. Simulation and Results.

STATCOM based on FLDCMC using PSC-PWM and FS-MPC control strategies are adopted and compared for compensating the voltage and the reactive power of the grid described in Figure 2. The grid parameters listed in Table 2 are used to configure the system. Simulation process has been performed to test the performance of the grid from the voltage, active and reactive power (P and Q) points of view. The grid behavior without applying STATCOM is shown in Figure 8. The effect of applying of STATCOM using PSC-PWM technique and STATCOM using FS-MPC technique at the behavior of grid have been illustrated in Figures 9 and 10, respectively.

Table 2. Grid parameters

Three Phase AC Source	
Rated voltage	33e3*1.0491kv
Frequency	50 Hz
S.C level	500 MVA
Power Transformer	
Primary voltage	33kv
Secondary voltage	11kv
Magnetizing resistance	500 p.u
Magnetizing inductance	500 p.u
Three Phase Load	
Load1	11MW, 10Mvar
Load2	11 MW, 10Mvar
Line length	5 km
The data of STATCOM	
Rated voltage	11kv
The capacitance of DC capacitors	480 mF
S.C level	100 MVA
Sample time Ts	15 μ sec.

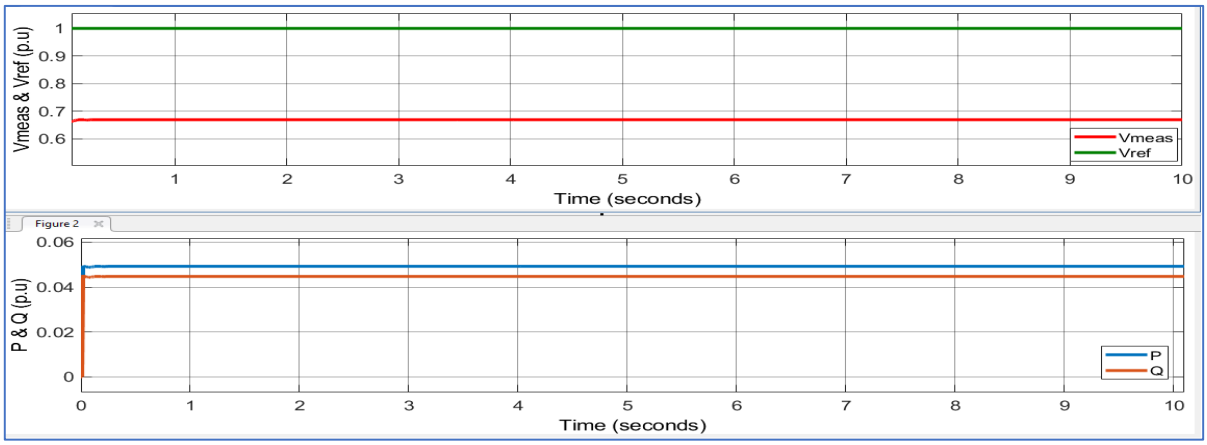


Figure 8. The grid behavior without STATCOM

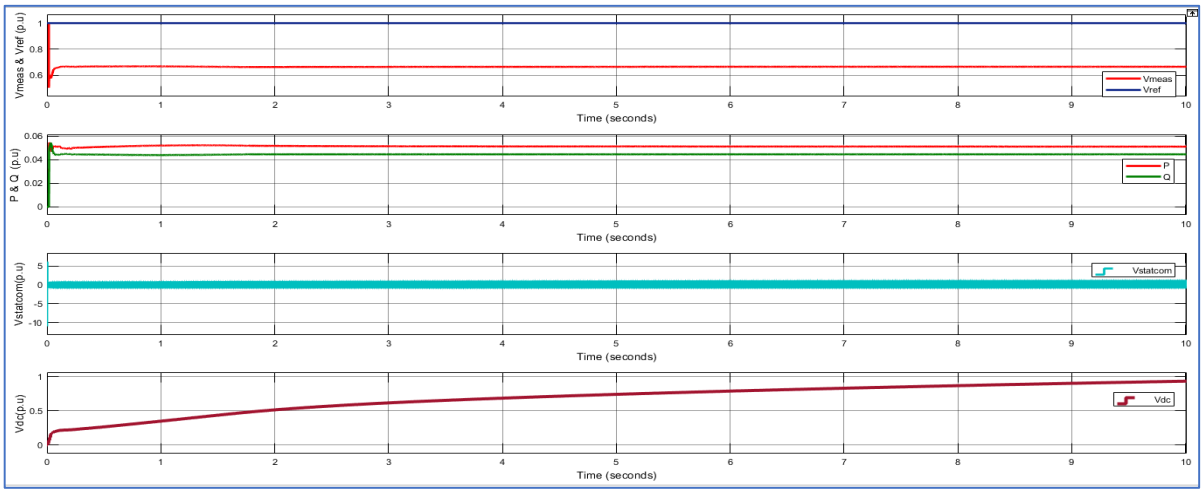


Figure 9. STATCOM using PS-PWM behavior

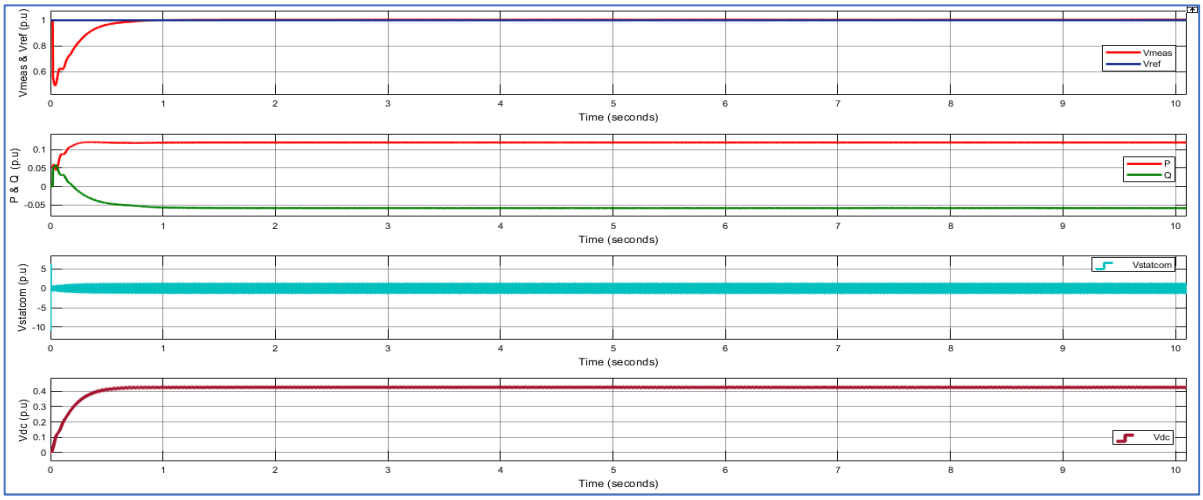
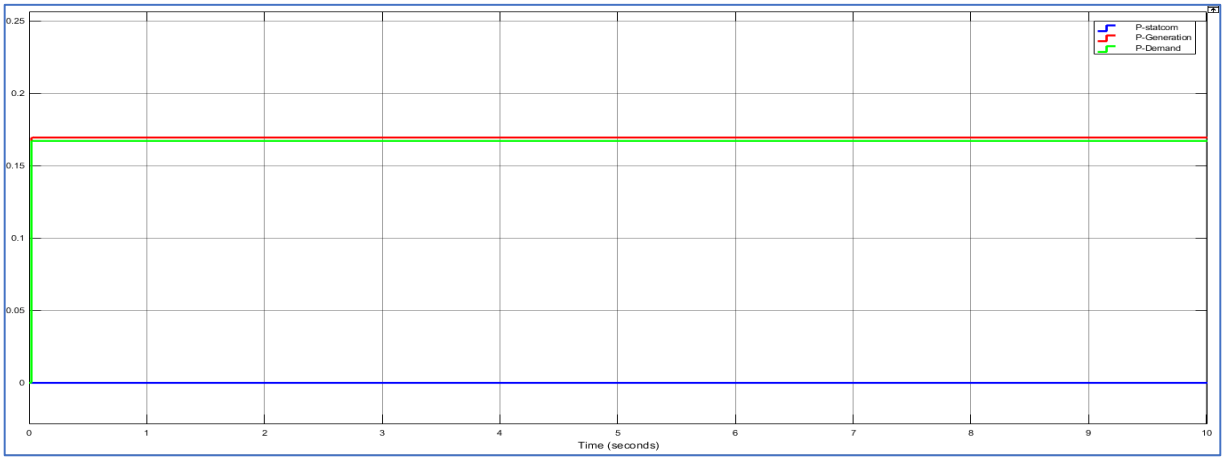
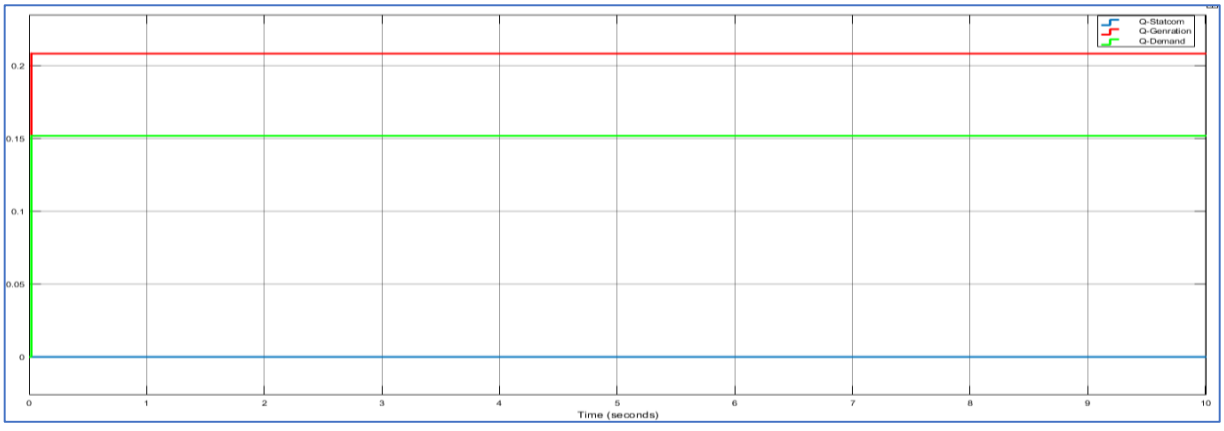


Figure 10. STATCOM using FS-MPC behavior

The grid behavior without applying STATCOM is shown in Figure 8, it can be observed that the measured voltage before applying the STATCOM at Bus 3 (Vmeas) is 0.67 p.u , P=0.0492 p.u & Q= 0.045 p.u. These data indicate the need to improve network voltage by compensating for reactive power using the STATCOM. Employing the STATCOM with PSC-PWM controller did not improve network performance effectively as shown in Figure 9, this is because the reactive power compensation was not sufficient to improve the voltage as required. On the other hand, the use of the STATCOM with FS-MPC controller contributed to the effective improvement of the network voltage as shown in Figure 10, and this is because a sufficient reactive power exchange was achieved.
Active and reactive power for generation, demand (Load) and STATCOM (P-generation, P-Demand, P-STATCOM) & (Q-generation, Q-Demand, Q-STATCOM) are illustrated in Figure 11 for the grid without STATCOM. Figure12 shows the aforementioned parameters for the grid with STATCOM using PSC-PWM, and Figure13 for the grid with STATCOM using FS-MPC.



(a)



(b)

Figure 11. Power for generation and demand without STATCOM (a) active power (b) reactive power

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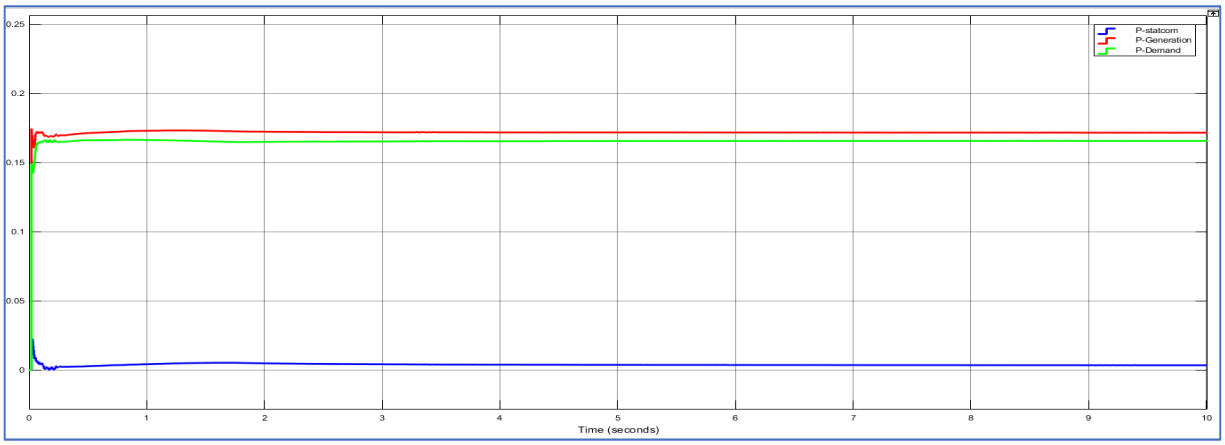
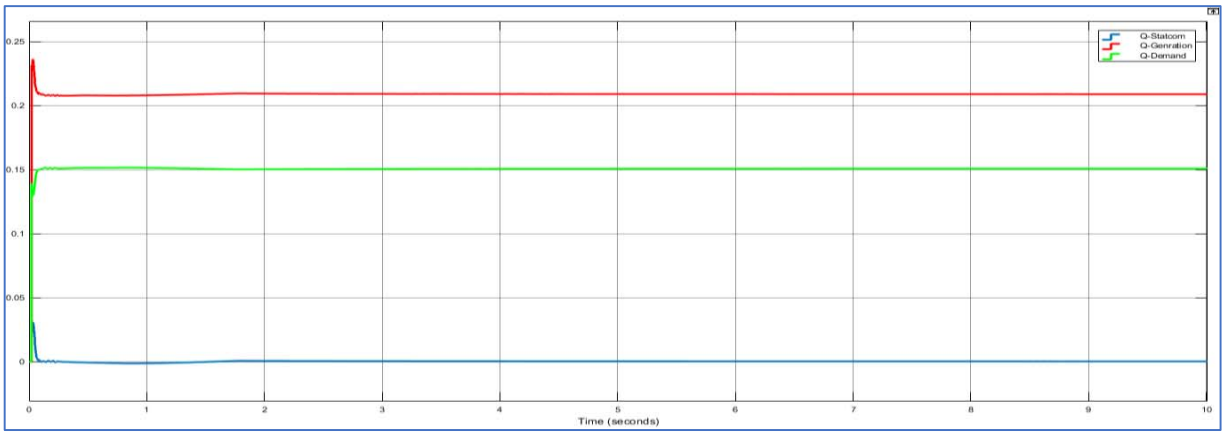
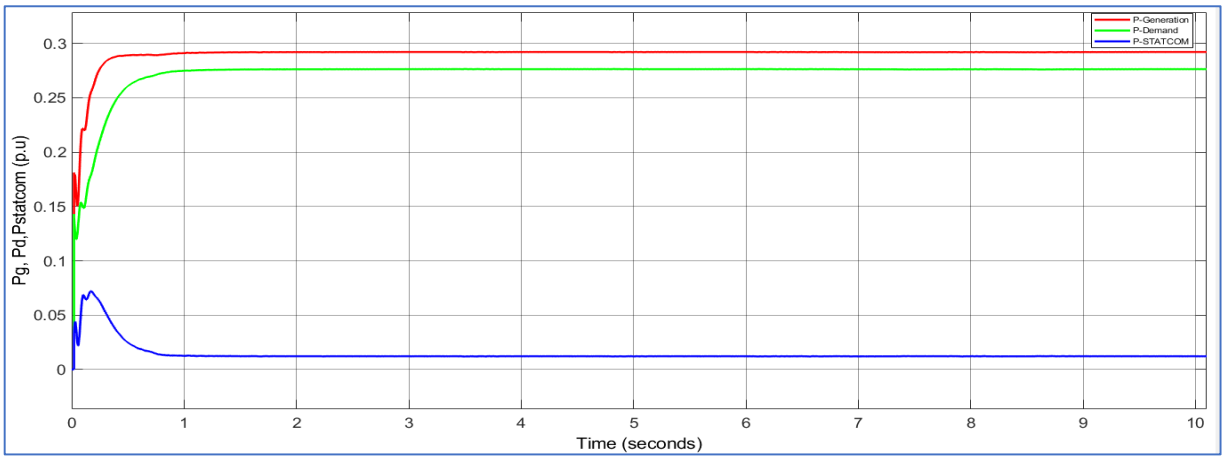


(a)

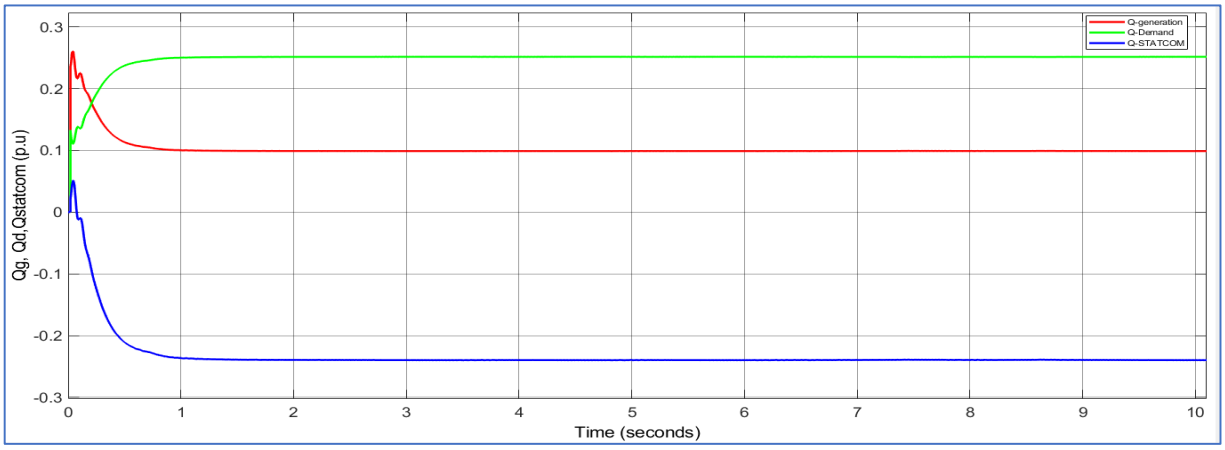


(b)

Figure 12. Power for generation and demand with STATCOM using PSC-PWM (a) active power (b) reactive power



(a)



(b)

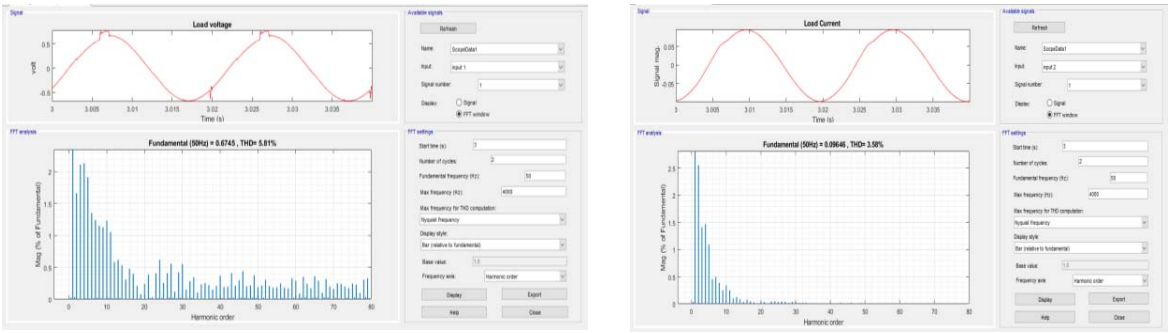
Figure 13. Power for generation and demand with STATCOM using FS-MPC (a) active power (b) reactive power

The behavior of the power system from the generated and demand power (active and reactive) points of view have been examined. Figure 11 shows the comparison between the generated and demand power when the STATCOM excluded. It can be noticed that the demand for reactive power needs to be strongly compensated. A slight compensation of the demand reactive power has been obtained when the STATCOM with PSC-PWM control algorithm is used as shown in Figure 12. A STATCOM with FS-MPC provides a significant compensation of the demand reactive power as shown in Figure 13. Table (3) summarizes the numerical results of the active and reactive power at the three sides (STATCOM, generation and load) for each case.

Table 3. Active and Reactive Power of the Power system

Case	Generation		Demand		STATCOM	
	P (p.u)	Q (p.u)	P (p.u)	Q (p.u)	P (p.u)	Q (p.u)
Without STATCOM	0.2083	0.1694	0.1668	0.1518	-	-
STATCOM with PSC-PWM	0.209	0.1715	0.165	0.15	0.0018	0.001
STATCOM With FS-MPC	0.292	0.1	0.276	0.25	0.0698	0.103

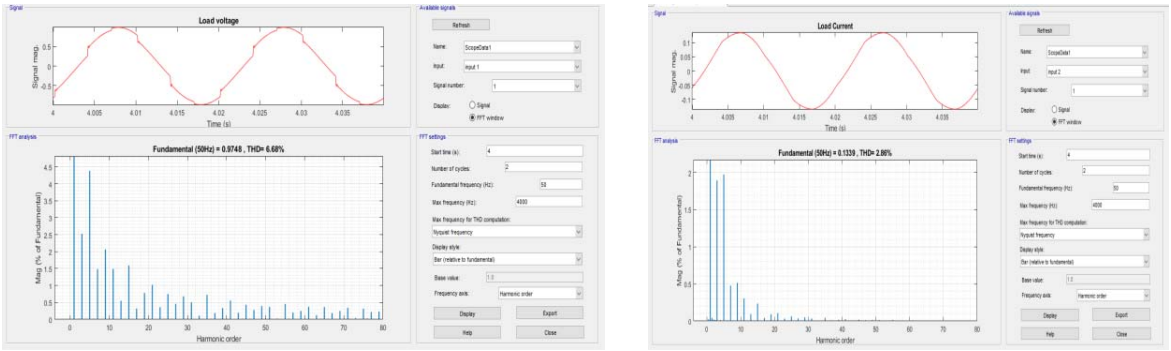
Figure 14 shows the total harmonics distortion (THD) of the voltage and current produced by the STATCOM when the PSC-PWM control strategy is used, while Figure 15 shows the THD of the voltage and current produced by the STATCOM when the FS-MPC control strategy is used.



(a) **(b)**

Figure 14. THD for STATCOM using PS-PWM

The THD of the load voltage when using STATCOM with PSC-PWM is higher about 1.01% compared with that when using STATCOM with FS-MPC. Moreover, the THD of the load current when using STATCOM with FS-MPC is less about 0.37% compared with that when using STATCOM with PSC-PWM.

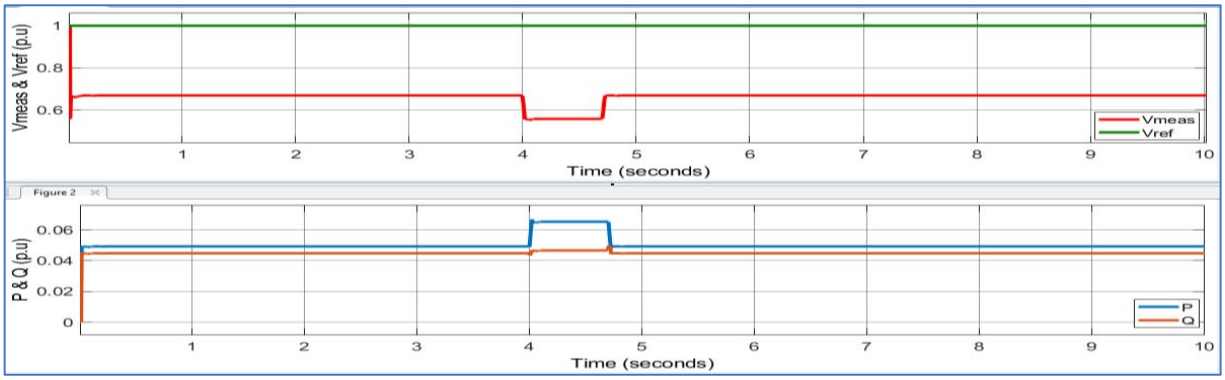


(a) **(b)**

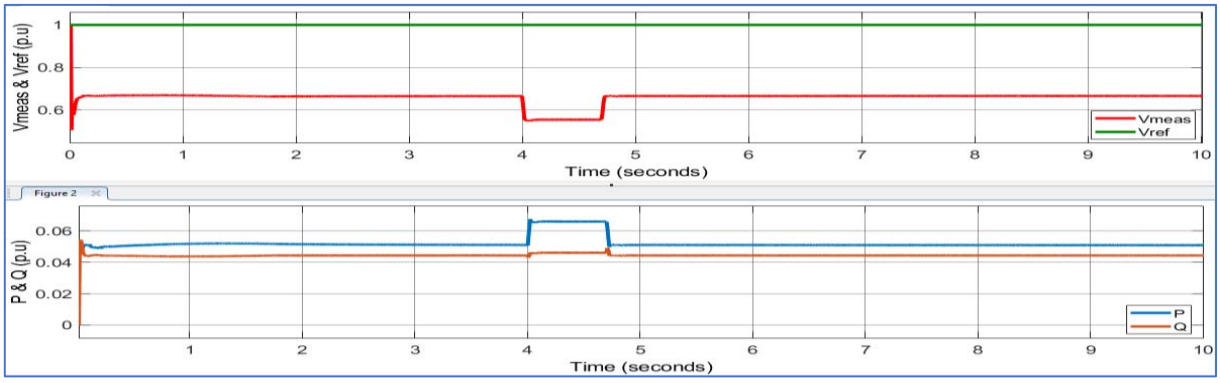
Figure 15. THD for STATCOM using FS-MPC

Moreover, the behavior of the STATCOM using the two control strategies is tested and compared in three cases: Load disturbance, two-phase to ground fault, and source disturbance.

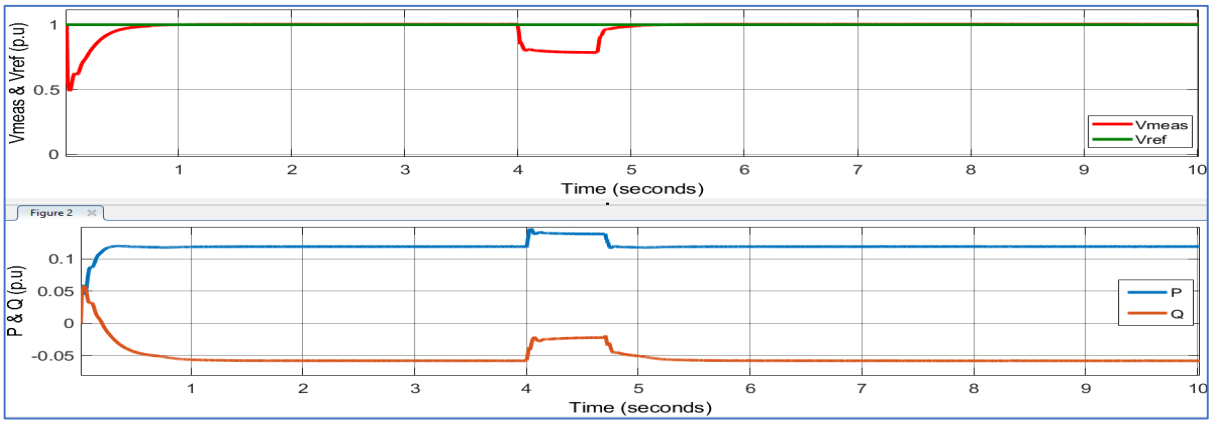
1.Case-study 1: The suggested grid overloaded by additional inductive load of (10MW, 5MVAR) connected to bus 3 via a circuit breaker at limited time between 4 to 4.7 second and the results shown in Figure 16.



(a)



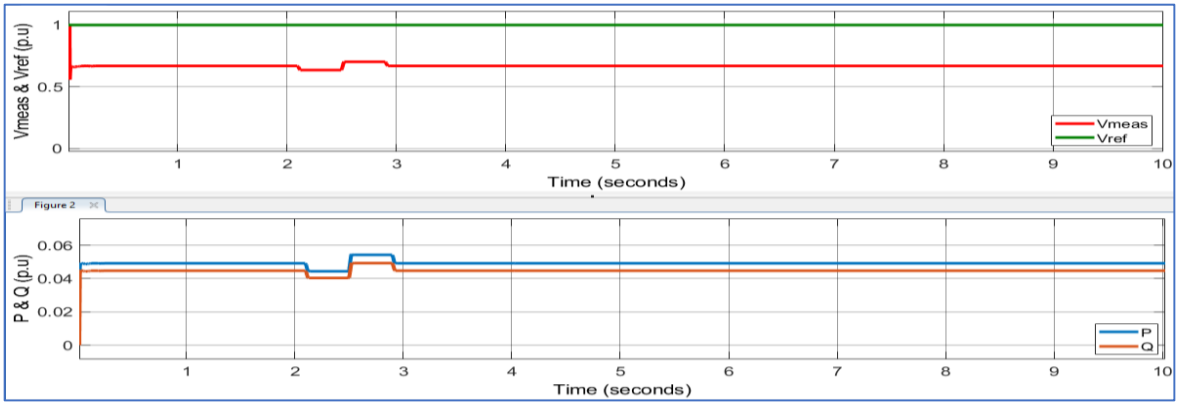
(b)



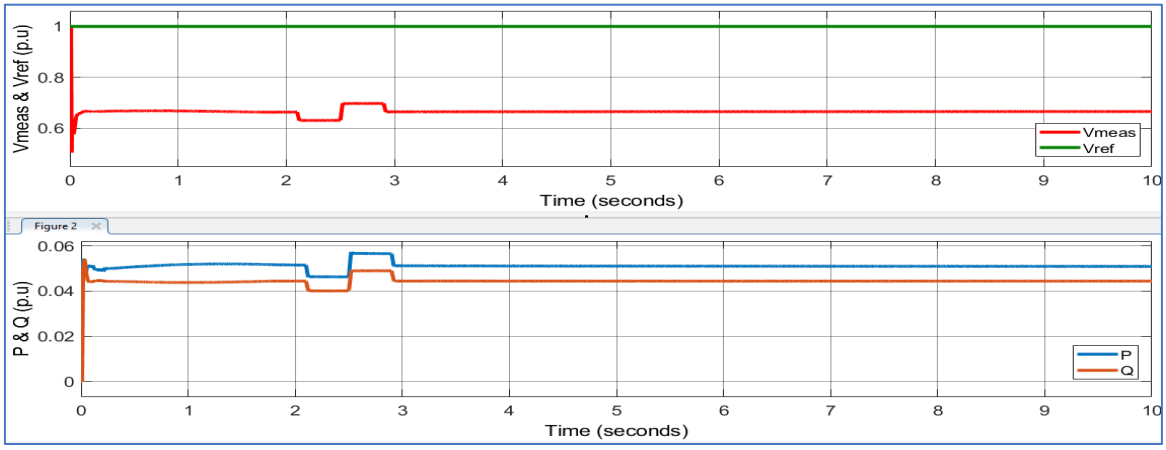
(c)

Figure 16. Effect of Load disturbance at the grid (a) without STATCOM (b) with STATCOM using PS-PWM (c) with STATCOM using FS-MPC

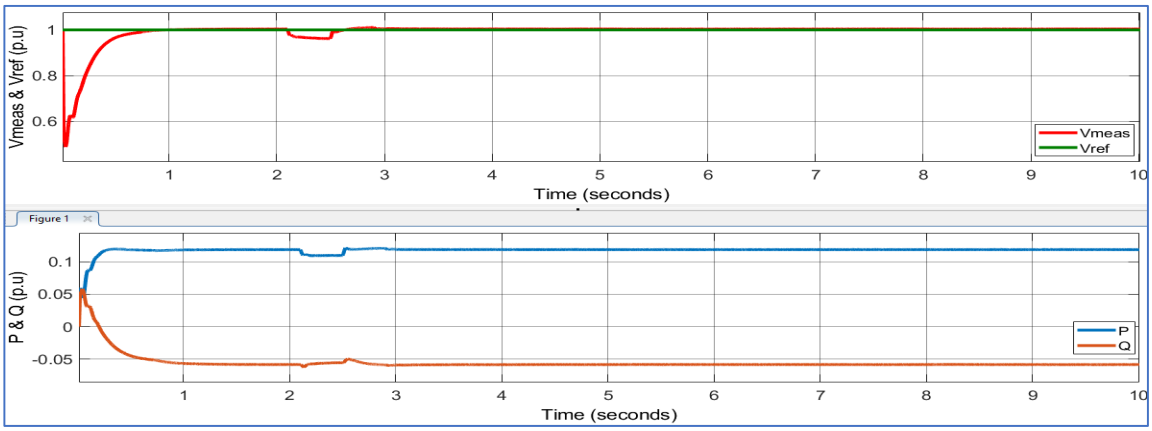
Case-study 2: the suggested grid is located under source disturbance where magnitude of the voltage is decreased to 0.95 pu in intervals between 2.1and 2.5 second. Then the magnitude of voltage increased to 1.01pu in durations between 2.5 and 2.9. as shown in Figure 17.



(a)



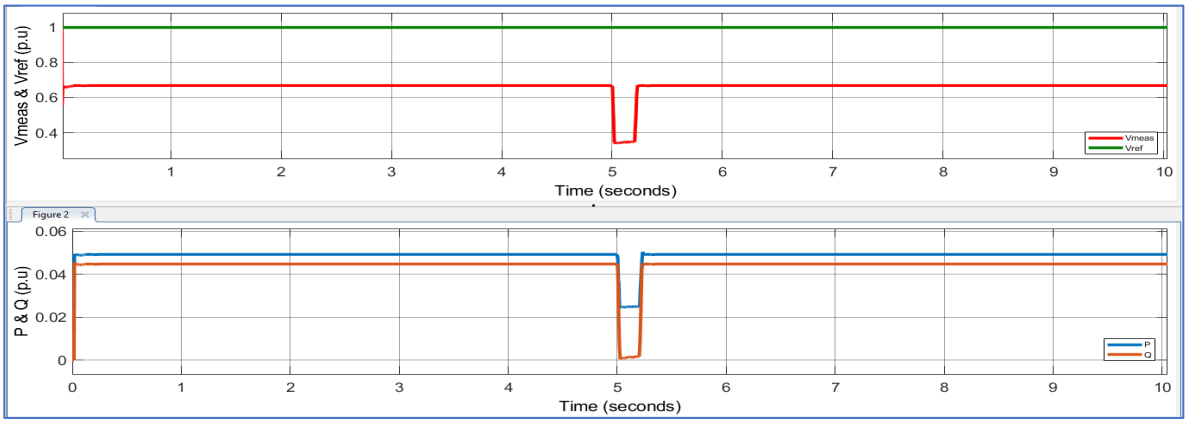
(b)



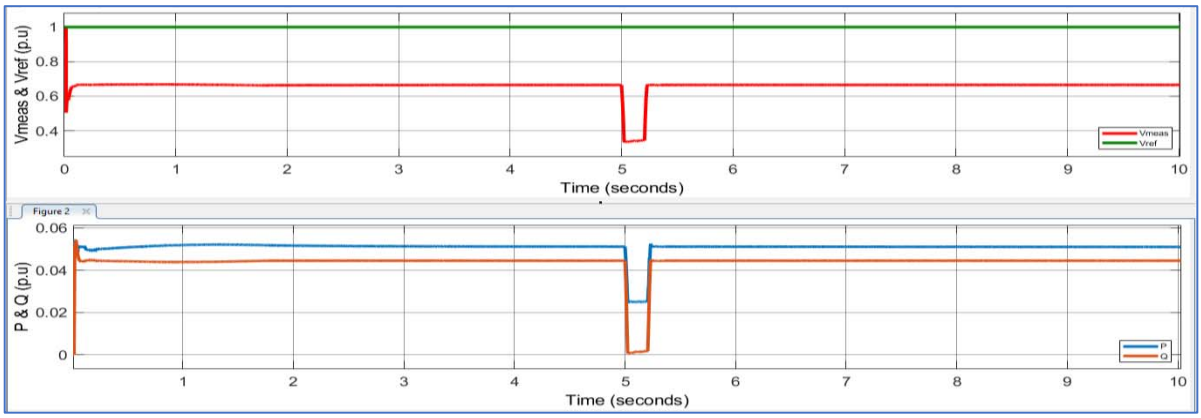
(c)

Figure 17. Grid with source disturbance (a) without STATCOM (b) STATCOM using PSC-PWM (c)with STATCOM using FS-MPC

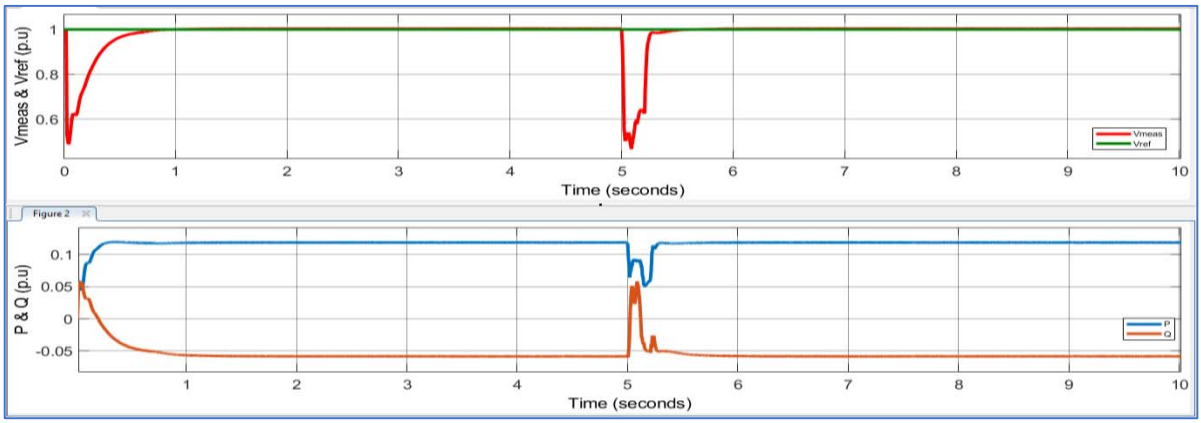
Case-study 3: the supposed grid is located under Single-Phase to Ground fault for the intervals between 5-5.2 sec. from the results shown in Figure 18 it is obviously that the STATCOM using FS-MPC is more effective in the fault duration.



(a)



(b)



(c)

Figure 18. Grid at fault case (a) without STATCOM (b) with STATCOM using PS-PWM (c) with STATCOM using FS-M

The results obtained from the study of the above three cases and shown in the Figures 16a, 17a and 18a confirm the necessity of using the STATCOM. Once again, the results show that the use of the STATCOM with PSC-PWM controller did not provide sufficient adaptation to the sudden changes occurred in the grid as shown in Figures 16b, 17b and 18b. Employment of the STATCOM with FS-MPC controller provides a significant adaptation to the sudden changes occurred in the grid as shown in Figures 16c, 17c and 18c.

7. Conclusion

A STATCOM based FLDCMC is proposed to improve voltage stability for suggested power system. In this work, two controlling methods are proposed: PS-PWM &FS-MPC. The use of the Finite Set-Model predictive control strategy compared with the Phase shift Carrier-PWM significantly reduced the calculation and the complexity of the controller structure. Although, it requires fast processors to perform the prediction of the subsequent gating pulses. Besides, STATCOM using FS-MPC has the capability to reduce reactive power losses on the power system compared with STATCOM using PSC-PWM. The behavior of the STATCOM using the two control strategies is tested and compared in three cases: Load disturbance, single-phase to ground fault, and source disturbance. The results obtained show a considerable difference in the use of the STATCOM with the two control strategies and the FS-MPC achieved better results

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