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High Gain Non-Isolated DC/DC Converter Based On Voltage-Lift Cell

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ABSTRACT This paper is about a voltage-lifting (VL)series technique is used to describe a non-isolated DC-DC converter with high voltage gain. With the VL technique's implementation, a structure made up two inductors, two diodes and one capacitor make it possible for them to achieve substantially larger voltage transfer gains. Due to their symmetrical architecture, they utilize less energy and put less strain on active switches and diodes than circuits of similar complexity since they charge and discharge their inductors in parallel and in series at the same time. Using Matlab/simulations and experiments, we do a thorough examination of both the continuous CCM and discontinuous DCM conduction modes..

Keywords DC-DC converter, voltage-lifting (VL)series, high voltage gain etc.

I. INTRODUCTION

Many electrical equipment rely on DC to DC step-up converters. Large conversion ratios, high power densities, and great efficiency are all essential for these converters. Over the last several years, Luo converters [1, 2] have become more popular. These converters' switches, those are divided into two categories (isolated and non isolated), are controlled using pulse width modulation (PWM) methods. The first category includes (Isolated DC-DC converters) like half bridges, full bridges, fly backs, and push pulls, among others. high frequency transformers are employed in this type to produce high voltage gain by adjusting the transformer's turns ratio. High frequency transformers also have a number of drawbacks, including transformer leaking inductance causes expensive costs, high - voltage power switching and big losses . To mitigate this difficulty, an active clamp circuit or (non dissipative snubbed) is utilized, although this increases the size and expense of the converter and makes the control process more complicated [3]. Non isolated DC-DC converters, such as (LUO,SEPIC ,CUK, buck boost and boost converters, and so on, are the second kind. High-frequency signals are used in this case,

Because no transformer is utilized, non-isolated (DC-DC) converters are inexpensive, tiny, have minimal switching losses, and are more efficient [4].Luo converters have recently become increasingly popular due to their ease of operation as well as manage [5]. One of the most popular Luo converters is this one [5, 6]. Basic, re-lift, and triple circuits are the three kinds of circuits in this family [6]. In addition, in [6,] an extensive examination of the converter in various operating situations is presented. Recently, contemporary (*DC-DC*) conversion enhancement techniques have been presented in [7, 8], including switched-inductor cell (SL), switched-capacitor cell (SC), and voltage-lift (V L). The switched-capacitor (SC) is a device that allows in electronic circuits and switched inductor (SL) are effective approaches that are extensively used in electrical circuits to step-up or step-down voltage transfer ratio gain [9]. Furthermore, the voltage-lift (VL) technique is frequently employed in electrical circuits, with the goal of increasing voltage and improving the performance of standard (DC-DC) converters [10, 11]. In addition, a nonisolated boost (*DC-DC*) converter based on the (VL) method is provided in [12], which has a large Voltage output increases. [13] Represents the need for a more thorough examination of the converterin various forms. An other to increase the gain in the voltage transfer ratio is to use the voltage-lift approach on a boost converter with a split inductor design. Despite this approach achieved a large increase in the voltage transfer ratio, this circuit has several electricity components and a total of four toggle switches, making it difficult to regulate, more expensive, and larger in size, and necessitating the use of contemporary ways to keep it under control[14]. In[15], a transform less (*DC-DC*)higher voltage transfer ratio improvement may be achieved with a simple circuit employing a voltage to current converter, however this circuit has the problem of being unable to give extremely gain in the transmission of voltage.

Other method for achieving increase in voltage transfer efficiency is described in [16]. The voltage multiplier for diode capacitors is a method that is based on ('Cockcroft-Walton and Dickie')are two frequent schemes. This technology is also used in the converter boost ,and it operates with a fast frequency of changeover switching.

Anovel technology so it uses Bootstrap Capacitors and Boost Inductors to create high voltage Boost Converters is described in [17]. PID is a pengendali programme in malaysia umpan balik that is often used in industrial systems. In order to drive the switch, a PID pengendali secara diskrit menghitung nilai kesalahan sebagai beda antara set point yang diinginkan and variabel proses terukur[18].

The anode of the diode connection location is changed to create this approach. The disadvantage of such a converter is that it has the two separate circuit, which makes it very difficult, larger, expensive, and creating substantial losses.

The use of a single switch non-isolated(DC-DC) converter has been presented in [19] as a current approach of boosting voltage ratio gain. The switchedinductor cell (SL), switchedcapacitor cell (SC) are combined to make this converter "as well as an additional boost capacitor

An alternate technique for getting a high voltage transfer ratio is described in [20], which involves replacing using a changed inductor unit in the new converter's new inductor (SL).

Each and every one articles listed in addition offered to demonstrate numerous proposals for boosting voltage utilizing various strategies and methodologies.By replacing the inductor with a switching capacitor inductor cell, this study provides a novel design and better adaptation of the new converter. Two inductors, two diodes and one capacito make up this construction. The use of a single switch for control is a key feature of the brand-new device.

Furthermore, the most latest converter is controlled just by one control circuit, This is voltage mode management using pulse width modulation(PWM). The new converter's analyses continuous and discontinuous modes of condition (*CCM*) and (*DCM*) is displayed. The latest converter is here also has a high voltage transfer ratio increase.

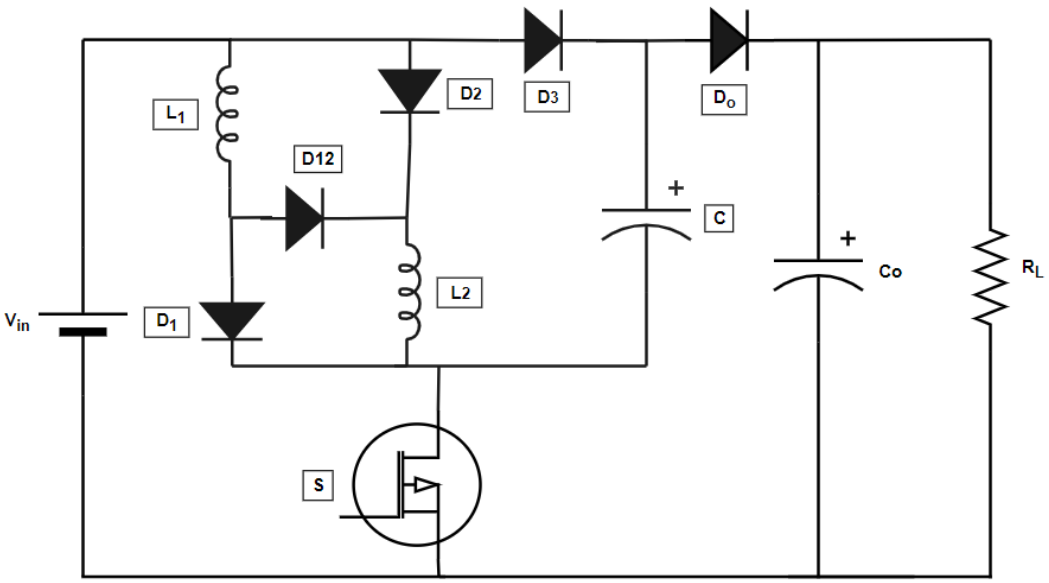
This paper is organized as follows: The first segment introduces a new converter modification. The second portion introduces the new converter's analysis. In part three, you'll learn how to create circuit elements. The management strategy is provided in part four. The pilot project data are reported in part five, and the conclusion is offered in section six.

II. PROPOSED DC-DC CONVERTER BASED ON VOLTAGE LIFT CELL AND DC EVALUATION

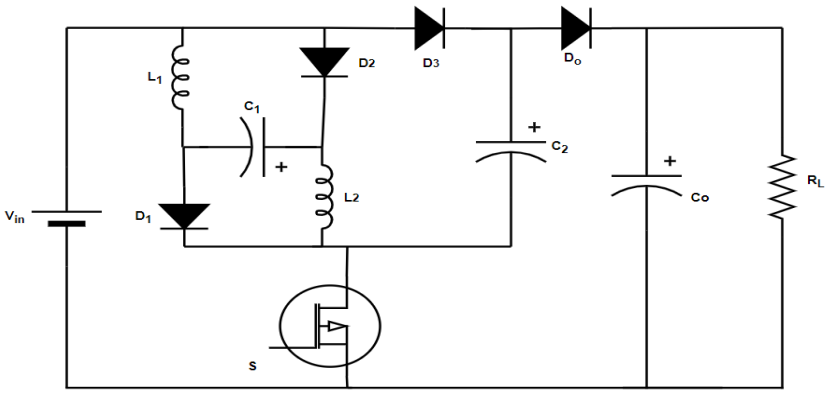
The fundamental converter is referred to as (Figure.1A) and a new converter is released (Figure.1B).The switched capacitor-inductor cells, which construction with components of two inductors(L_1 and L_2) , two diodes (D_1 and D_2) and one capacitor(C_1), replaces the converter's inductor (L) . Magnetic coupling exists between inductors (L_1 and L_2) (non- isolated). The following assumptions should be considered In order to make DC analysis more straightforward:The following conditions: I) all passive and active components are excellent; ii) all capacitors are large enough, and the voltage across capacitor is constant; and, iii) the DC analyses of the converter is in stable state, which means that the results are consistent. Furthermore, we assume that the inductors are equivalent in order to decrease ripple.

$$V_{in} = VL_1 = VL_2$$

The inductance of the inductors is represented by (L).



A



B

Figure 1. There are two variants of converter **: A -** The most basic converter B- Its suggested improved converter based on voltage lift cell

In addition (In this scenario, the windings are put to better use.). We also suppose $L_1 = L_2 = L$. The basic type converter's voltage transfer ratio (Fig. 1A) is as follows:

$$\boldsymbol{G_D = \frac{V_o}{V_{in}} = \frac{2}{1-D}} \quad (1)$$

D denotes the power switch's duty cycle.

The voltage transfer ratio approaches that of a traditional boost converter quantitatively for large values of duty cycle D.

The performance of a novel converters in the three methods (CCM, DCM, and BCM) as well as the boundary operation conduction type (BCM) between the two methods (CCM, DCM) is examined in this section.

A. CCM analysis

When the $\boldsymbol{CCM}$ is in a condition of equilibrium, the proposed circuit's switching topologies (Fig. 1B) are presented in Figures (2A and 2B) as well as the time switches that corresponds to it is shown in(Fig. 3). There are two methods of operation for the converter's switches: first, and second.

1. first : *[t0, t1].* It everything begins at $[t_0 . t_1]$. See Figures (2A) and(3).The switch has been flipped (ON)at (t_0). The diodes link two capacitors, $(C_1 and\ C_2)$, and two inductors $(L_1$ and $L_2)$, in parallel to the voltage source (V_{in}) $(D_1$, $D_2 and\ D_3)$. The diodes $(D_1$, $D_2 and\ D_3)$. are in forward mode throughout this time, At this moment, the diode (D o) is operating in reverse mode. At this moment, the diode (D_o) is operating in reverse mode.

2. second : $[t_1 . t_2]$. This is the mode begins at $[t_1 . t_2]$ (Figures. 2B and 3). At time (t_1), the switches (S) is activated (OFF).The diode now connects the two capacitors $(C_1 and\ C_2)$, The two inductors $(L_1\ and\ L_2)$, as well as the source voltage (Vin), The diode is in series with the capacitor (C_o) and the load ($\boldsymbol{Do}$). The diode ($\boldsymbol{Do}$) is set to forward throughout this time, while the diodes $(D_1$, $D_2 and\ D_3)$ are in reverse mode.

First, we'll go over the new converter circuit's voltage transfer gain ratio (G_D) in the (CCM) mode.

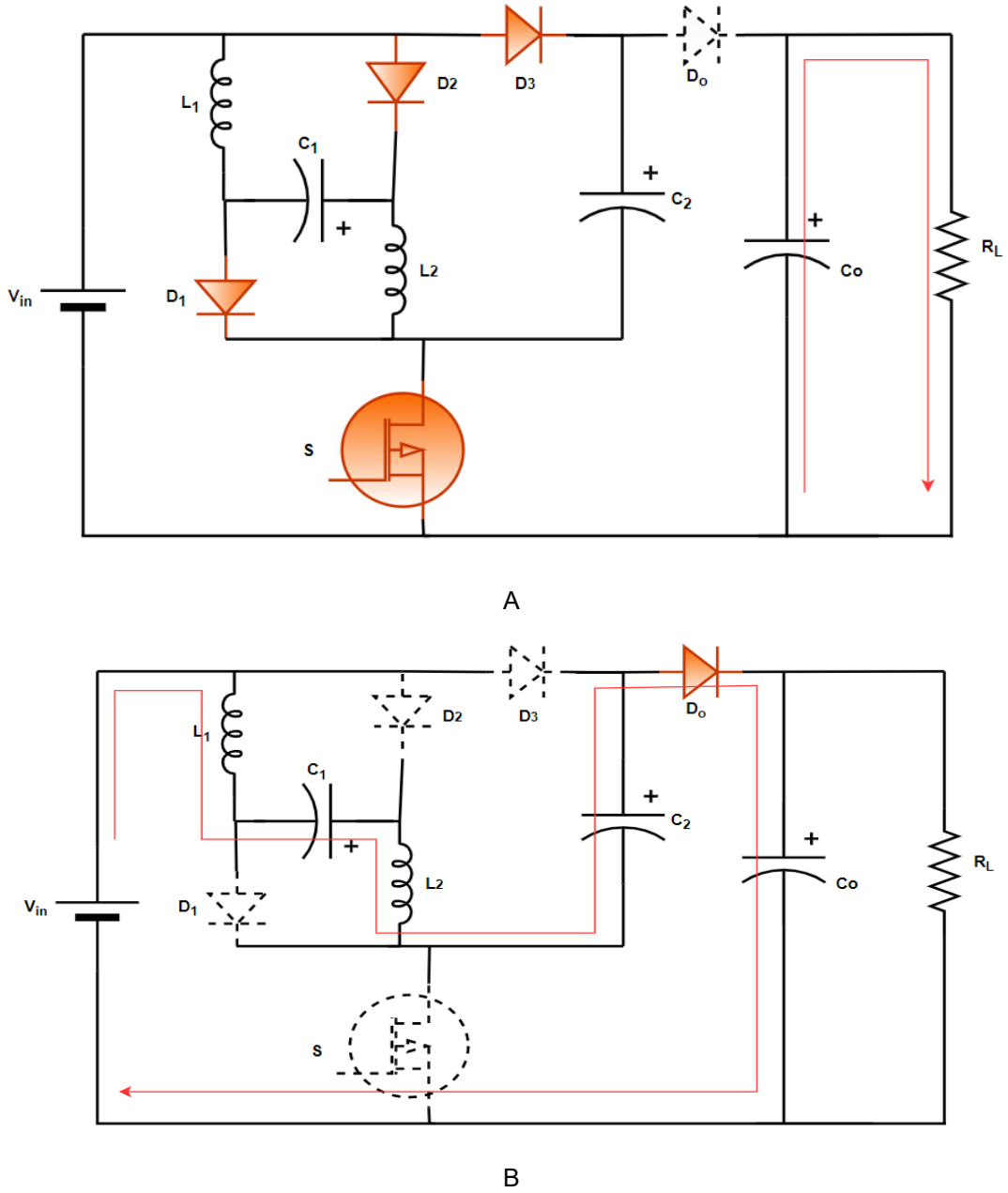


Figure 2: shows the proposed circuit's switching stages. A : t_{ON}, and B : t_{OFF}

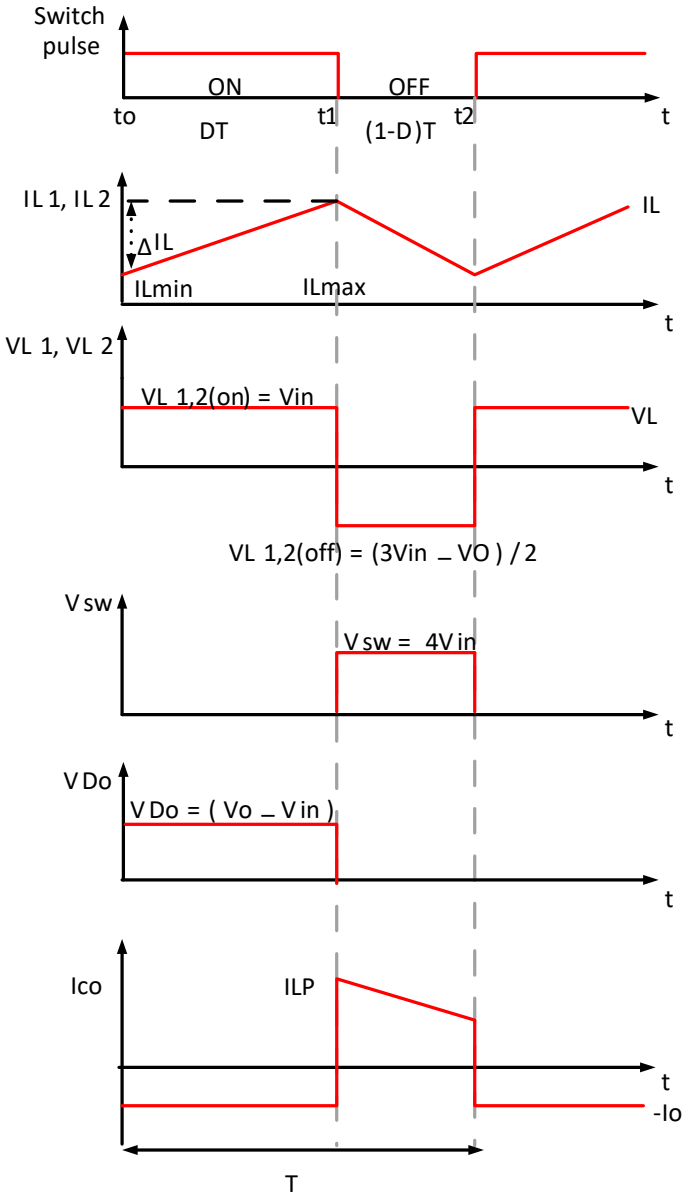


Figure 3: Proposed CCM converter switching schematic

At the switching (***ON***) period **(** $t_{ON} = D\,T$ **)**

$$\mathrm{Vin} = \mathrm{VL1-ON} = \mathrm{VL2-ON} = \mathrm{VC1} = \mathrm{VC2} \quad (2)$$

And at the switching (***OFF***) period **(**$t_{OFF} = (1-D)T$ **)**

$$\mathrm{Vin} - \mathrm{VL1-OFF} - \mathrm{VL2-OFF} + \mathrm{VC1} + \mathrm{VC2} - \mathrm{Vo} = 0 \quad (3)$$

This gives us the following results:

$$\mathrm{V_{L1-OFF}} = V_{\mathrm{L2-OFF}} = \frac{3\,V_{in}-V_O}{2} \quad (4)$$

We get the following results using the voltage - second balance equation across the inductors (L_1 and L_2):

$$\int_0^{DT_S} \mathrm{V_{L-ON}}\,\mathrm{dt} + \int_{DT_S}^{T_S} \mathrm{V_{L-OFF}}\,\mathrm{dt} = 0 \quad (5)$$

$$\mathrm{V_{L-ON}\,D\,T} + \mathrm{V_{L-OFF}\,(\,1-\,D\,)\,T} = 0 \quad (6)$$

The following is an expression for the relationship between the voltage transfer ratio and equation (6):

$$\frac{V_o}{V_{in}} = \frac{3-D}{1-D} \quad (7)$$

The new converter circuit in (CCM), (G_D), has a voltage gain ratio of:

$$\boldsymbol{G_D = \frac{V_o}{V_{in}} = \frac{3-D}{1-D}} \quad (8)$$

The input and output powers of ideal components are identical, hence the input current may be calculated as follows:

$$\boldsymbol{I_{in} = \frac{3-D}{1-D}\ I_o} \quad (9)$$

During the [$t_1 . t_2$] period (switching-OFF), the charge (Q) of the capacitor (Co) grows, and during the [$t_0 . t_1$] period (switching-ON), it drops. We are in possession of

$$\mathbf{Q_{Co+}} = \mathbf{I_o\ D\ T}$$

$$\mathbf{Q_{Co-}} = \mathbf{I_{Co-off}\ (1\ -\ D)\ T} \quad (10)$$

During the ON/OFF switching cycles ($\mathbf{Q_{Co+}} = \mathbf{Q_{Co-}}$). As a result of equation ten, we obtain:

$$\mathbf{I_{Co-off}} = \frac{D}{1-D}\ \frac{V_o}{R} \quad (11)$$

($I_{Do} = I_{Co} + I_o$) at the **[$t_1 . t_2$]** time (switching-**OFF**). Thus**,**

$$\mathbf{ID_{o-off}} = \mathbf{I_{Co-off}} + \mathbf{Io} \quad (12)$$

$$\mathbf{ID_{o-off}} = \frac{1}{1-D}\ \boldsymbol{I_o} \quad (13)$$

Furthermore, during the **[$t_1 . t_2$]** phase (switching- **OFF**), C1,C2, L1and L2 become series linked, enabling them to use $\mathbf{D_o}$ as a means of discharging stored energy into the load.Therefore,

$$\mathbf{I_{L1}} = \mathbf{I_{L2}} = \mathbf{I_{C1-off}} = \mathbf{I_{C2-off}} = \mathbf{ID_{o-off}} = \frac{1}{1-D}\ \boldsymbol{I_o} \quad (14)$$

During both switching cycles, $\mathbf{Q_{C1+}} = \mathbf{Q_{C1-}}$, $\mathbf{Q_{C2+}} = \mathbf{Q_{C2-}}$Therefore,

$$\mathbf{I_{C1-off}\ (1\ -\ D)\ T} = \mathbf{I_{C1-on}\ D\ T}$$

$$\mathbf{I_{C1-on}} = \frac{1-D}{D}\mathbf{I_{C1-off}} = \frac{1}{D}\ \boldsymbol{I_o} \quad (15)$$

$$\mathbf{I_{C2-on}} = \frac{1-D}{D}\mathbf{I_{C2-off}} = \frac{1}{D}\ \boldsymbol{I_o} \quad (16)$$

Since $L_1 = L_2 = L$, the (peak-peak) current variation of the inductor (Δi_L), Δi_L is equal to ($\Delta \boldsymbol{i_l} = \frac{D\ T\ V_{in}}{L}$), where the current variation ratio is (δ_l), and since$L_1 = L_2 = L$. So;

$$\boldsymbol{\delta_l} = \frac{\frac{\Delta i_l}{2}}{I_L} = \frac{D\ T\ V_{in}}{2L\ I_L} = \frac{D\ (1-D)}{G_{CCM}}\ \frac{R}{2\ f\ l} \quad (17)$$

As a result of equation (17), the current variation ratios in inductors ($L_1 and\ L_2$) are as follows:

$$\boldsymbol{\delta_{L1}} = \boldsymbol{\delta_{L2}} = \boldsymbol{\delta_L} = \frac{\frac{\Delta i_l}{2}}{I_L} = \frac{D\ T\ V_{in}}{2L\ I_L} = \frac{D\ (1-D)}{G_{CCM}}\ \frac{R}{2\ f\ l} \quad (18)$$

During the **[$t_1 . t_2$]** .(switching- **OFF**) period, The output diode's current fluctuation **($\Delta I_{D\,o}$)** is equal to the inductors' current variation **(ΔI_L).** As a result, the output diode current ($\boldsymbol{I_{Do}}$) variation ratio is ($\boldsymbol{\delta_{D\,o}}$)

$$\delta_{Do} = \frac{\frac{\Delta i_l}{2}}{\mathrm{ID_{o-off}}} = \frac{D\ (1-D)}{G_{CCM}}\ \frac{R}{2\ f\ l} \quad (19)$$

Because (L1 ≠ L2). a pulsating current ripple in an inductor changes derived in equations (17-19) the situation changes during the process of switching. During the switching-**OFF** time, the inductors($L_1 and\ L_2$) a sequence of energy discharges. Under high switching frequency,If the inductors ($L_1 and\ L_2$) are equivalent in capacitance, the current ripple will be reduced. If the inductors ($L_1 and\ L_2$) are equivalent in capacitance, the current ripple will be reduced.

($\Delta \boldsymbol{V_o} = \frac{D\ T\ I_o}{C_o}$) is the (peak-to-peak) variation of the output voltage (ΔV_o). As a result, the output voltage variation ratio ($\boldsymbol{\delta_{Vo}}$) equals:

$$\delta_{Vo} = \frac{\frac{\Delta V_o}{2}}{\mathrm{V_o}} = \frac{D\ T\ I_o}{2C_o\ V_o} = \frac{D}{2\ f\ R\ C_o} \quad (20)$$

III. DCM ANALYSIS

As illustrated in Figures 4 , the DCM analysis may be separated to one of three settings: first, second, and third.

1. first: This mode begins at **[$t_0 . t_1$]** . During this time, the switch (S) is switched on (**ON**), (Figure.2A) and the time diagram is provided in (Figure.3). **CCM** and **DCM** are identical in this mode of operation. Inductors ($L_1 . L_2$) have a current in inductors (ΔI_l) varies (peak-to-peak) as follows: Where (I_{LP}) stands for (peak-peak) current fluctuation in inductors, and

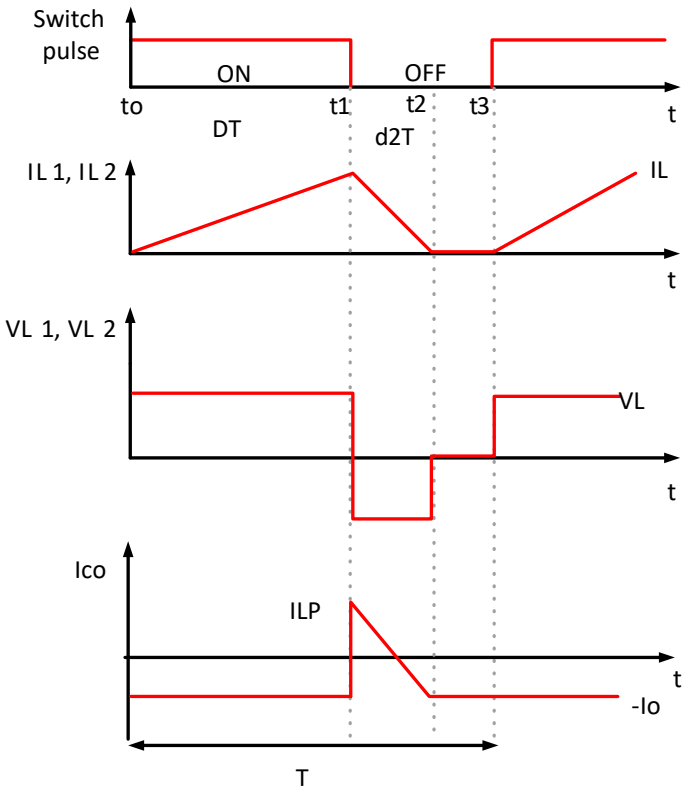
$$I_{LP1} = I_{LP2} = \Delta i_L = \frac{V_{in}\ D\ T}{L} \quad (21)$$

2. second: This mode begins at **[$t_1 . t_2$]** . During this time, the switch (S) is turned (OFF), is seen in (Figure .2B), and a time diagram is depicted in (Figure .4). The supply voltage is a device that produces voltage (Vin), $C_1 . C_2 . L_1\ and\ L_2$ are all linked in series to allow their stored energy to be released to**Co** and the weight on the system. Currents generated by inductors($\boldsymbol{I_{L1}} . \boldsymbol{I_{L2}}$) reach zero at ($\boldsymbol{t_1 = t_2}$). Another version of ($I_{LP1}\ and I_{LP2}$) is as follows:

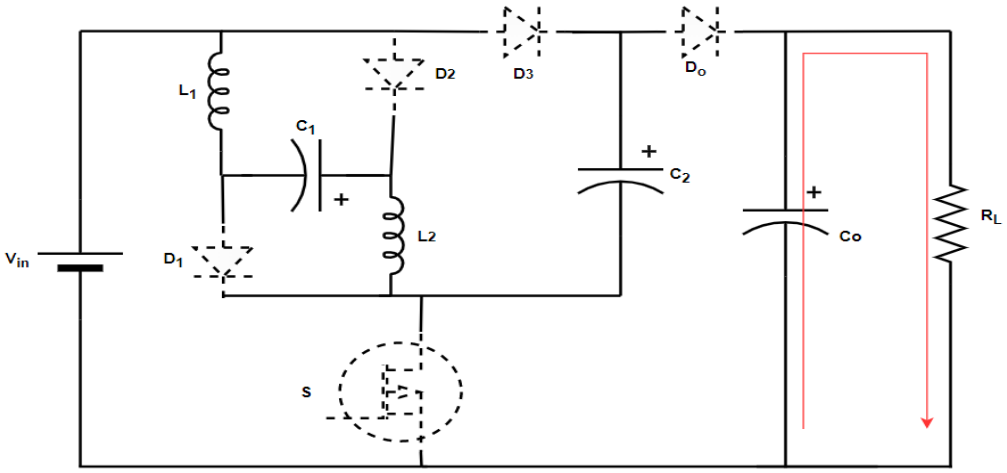
$$\boldsymbol{I_{LP1} = I_{LP2}} = \Delta \boldsymbol{I_L} = \frac{(V_o - 3\ V_{in})\ \ d2\ T}{2\ L} \quad (22)$$

3. third: This mode begins at **[$t_2 . t_3$]**. In this period, the switch (**S**) is still switched (**OFF**), as shown in (Fig. 5), and in which is indicated the matching timetable (Fig. 4). The accumulated energy in $\boldsymbol{L_1\ and\ L_2}$ become zero. As a result, just the stored energy in **Co** is transferred to the load. At steady state, the time period(**d2**) is derived by equating the two equations (21 and 22) as follows:

$$d_2 = \frac{2\,V_{in}\,D}{(V_o - 3\,V_{in})} \quad (23)$$



Figures 4 , Waveforms Typical of the New Converter in DCM



Figures 5. Steps to switch over to the new converter circuit at (DCM)

The average output-capacitor current(I_{Co}) as well as switching operations (ON)and OFF) may be found in (Fig. 4):

$$I_{CO} = \frac{\frac{1}{2} d_2\, I_{LP}\, T - I_O\, T}{T} = \frac{1}{2}\, d_2 I_{LP} - \; I_O \quad (24)$$

In equation (24), the output capacitor current (I_{CO}) reaches zero in steady state, yielding the following:

$$I_O = \frac{1}{2}\, d_2\, I_{LP} \quad (25)$$

We get the following by substituting (21) and (23) into (25) and ($I_o = \frac{V_O}{R}$):

$$\frac{V_O}{R} = \frac{V_{in}^2\, D^2}{f\, L\, (V_O - 3\, V_{in})} \quad (26)$$

The switch frequency is (f), and it equals (f= $\frac{1}{T}$), (τ_L) is the inductor's normalized time constant, which is calculated as follows: $\tau_L = \frac{f\,L}{R}$

In (DCM), (G_D) Specifies the voltage gain ratio of the circuit of the completely new converter:

$$G_{DCM} = \frac{V_O}{V_{in}} = \frac{3}{2} + \sqrt{\frac{9}{4} + \frac{D^2}{\tau_L}} \quad (27)$$

IV. BCM ANALYSIS

Boundary conduction mode is another way of operation for the new converter (**BCM**). The voltage ratio will be higher if the new converter is used in this method improvements of the (**CCM**)and (**DCM**) willbe equal. The inductor's boundary normalized time constant (τ_L) may be calculated using (8) and (27): $\boldsymbol{G_{CCM} = G_{DCM}}$

$$\boldsymbol{\tau_L = \frac{D\,(1-D)^2}{2\,(3-D)}} \quad (28)$$

In this diagram, the border between the two modes (CCM) and (DCM) is shown (fig. 6). Figure

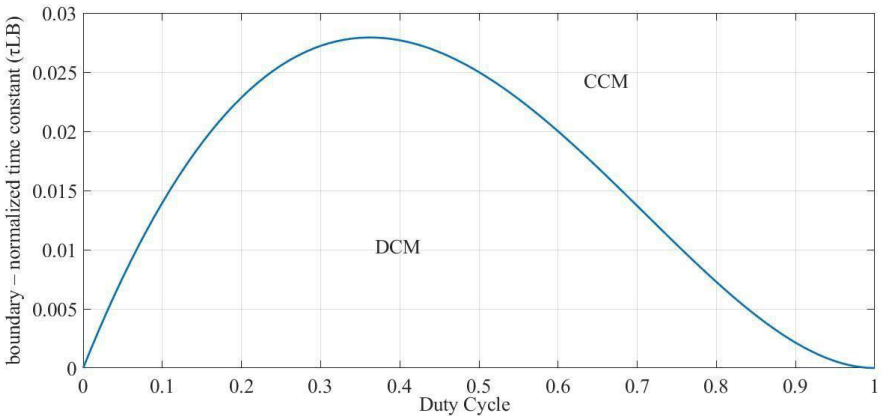


Figure 6: The line that separates the two modes (CCM) and (DCM)

V. ANALYSIS OF THE PLANNED CONVERTER ADJUSTMENT BASED ON VOLTAGE LIFT CELL

1. Inductors design

The inductors' values are chosen to be equal ($\boldsymbol{L_1 . L_2 = L}$) to make the new converter's ripple less noticeable As a consequence, if the current ripple ($\Delta \boldsymbol{I_L}$) and switch frequency(f) are considered to be constant, the value of the inductors may be calculated as follows:

$$\boldsymbol{I_{L1} = I_{L2} = \frac{D\,V_{in}}{f\;\Delta I_L}} \quad (29)$$

2. Capacitor design

The capacitor design is influenced by the switching frequency(f) and capacitor voltage ripple. ($\Delta \boldsymbol{V_C}$). As a result, we can calculate the output capacitor (**Co**) using equation (20):

$$\boldsymbol{C_o = \frac{D\,V_o}{f\,R\,\Delta V_C}} \quad (30)$$

Furthermore, The boosting capacitor values($\boldsymbol{C_1}$ and $\boldsymbol{C_2}$)may well be calculated:

$$\boldsymbol{C_1 = C_2 = \frac{I_{in}\,(1-D)}{2\,f\,\Delta V_C}} \quad (31)$$

Substituting eq. (9) for eq. (31) yields:

$$\boldsymbol{C_1 = C_2 = \frac{(3-D)\,V_o}{2\,Rf\,\Delta V_C}} \quad (32)$$

VI. CONTROLLING STRATEGY (THE VOLTAGE MODE CONTROL OF THE NOVEL CONVERTER)

Voltage mode control is the novel converters control method (VMC). Itprovides features suchas ease of use and efficiency. The load voltage (output voltage) is compared to a constant reference voltage in order for this approach to work. There is a disparity between the reference voltage and the voltage applied to the load (output). referred to as the voltage difference (error). The (PID)controller receives the generated error. The PID As illustrated in the figure, the controller and saturation ('Limiter') outputs are fed into the (PWM) to drive the switches (Figure.7).

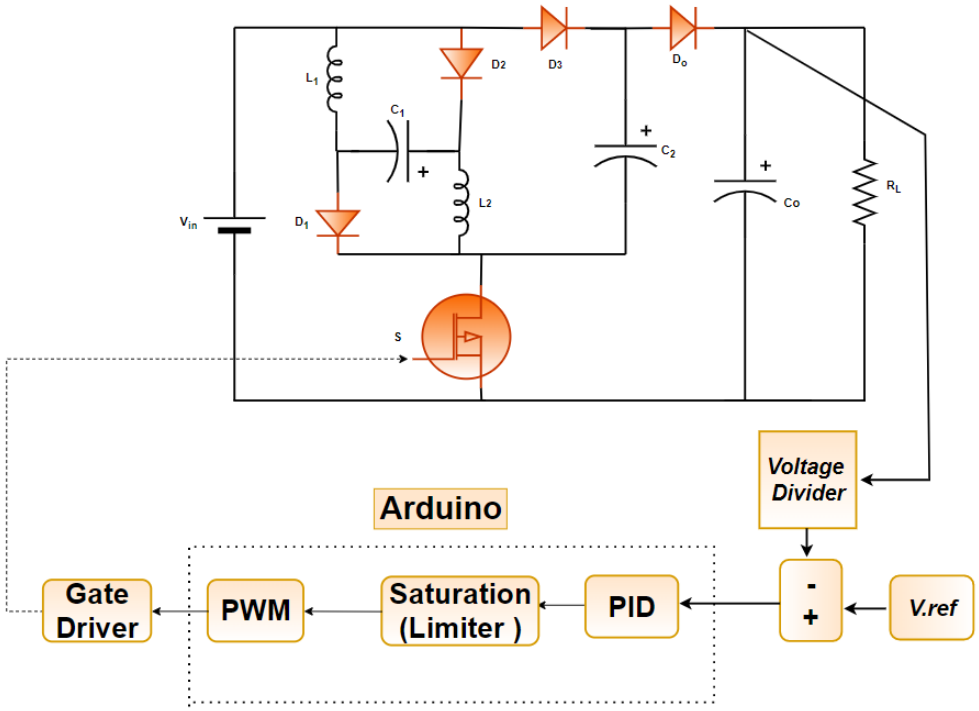


Figure 7 .shows the voltage mode. Controlling the switch

VII. THE RESULTS OF THE EXPERIMENT

The suggested converter's test parameters were designed using equations (29, 30, 31 and 32). As a result, the components employed in the design have the following values: Vin = 24 volts, f = 20 KH, and D = 0.5. The circuit's parameters are as follows: L1= L2 = 67 uH, C1 = C2 = 100u F, and Ro= 543 for the output resistance. The transistor utilized is an IRF 250 MOSFT transistor. depicts the suggested converter's supremacy when it comes to boosting voltage output transfer increase over the circuit.(Figure10) depicts the degree to which theoretically and experimentally findings are in accord, which is based on a practical comparison of outputand inputvoltage. Figure 6 represents the point at where continuous and discontinuous systems merge. Figure 13 confirms a voltage waveform over an inductor. The output and input voltages are compared in a simulation for the new converter, and the results are given in(fig. 8).

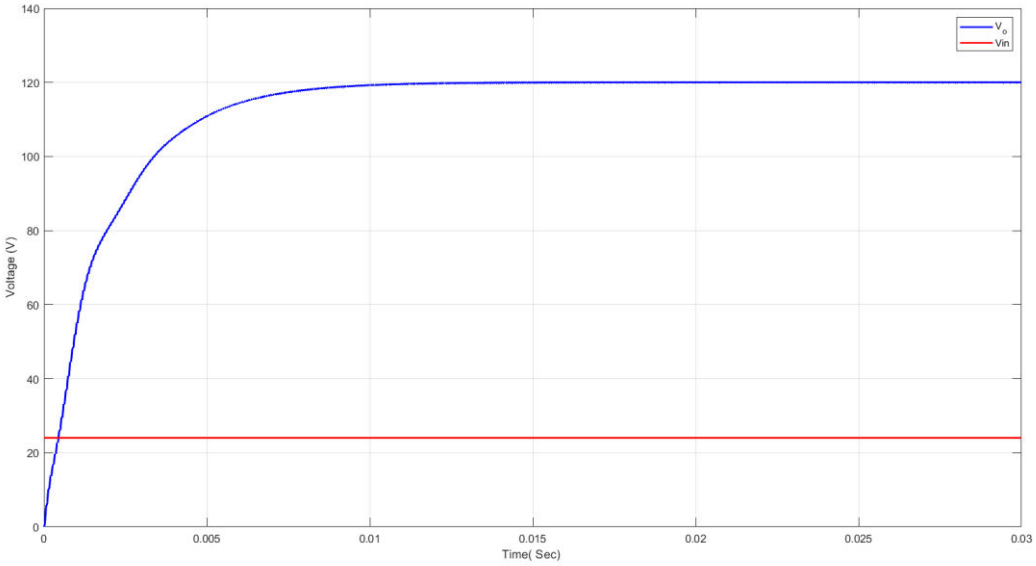


Figure 8: Voltage in this case, the output and the input are especially compared.

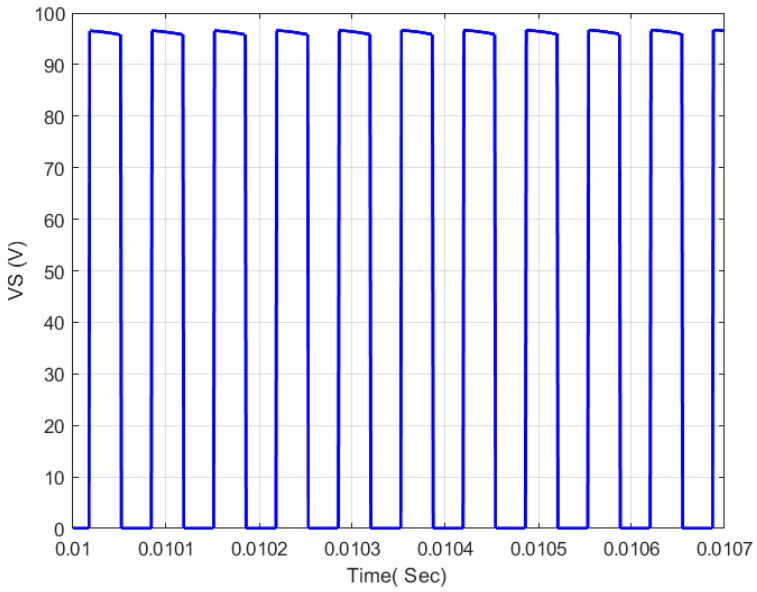


Figure 9: shows the MOSFET transistor's switching frequency in a computer game.

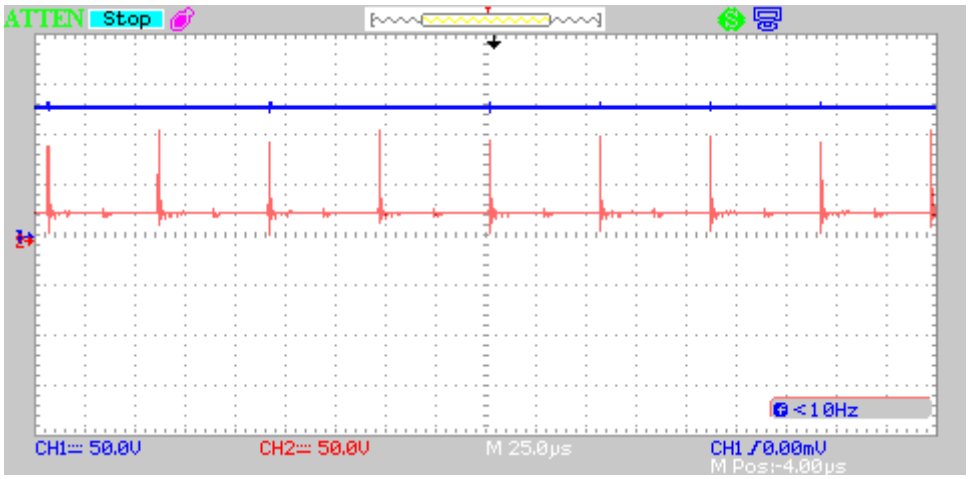


Figure 10: displays the experimental results of a realistic comparison of the output and input voltages.

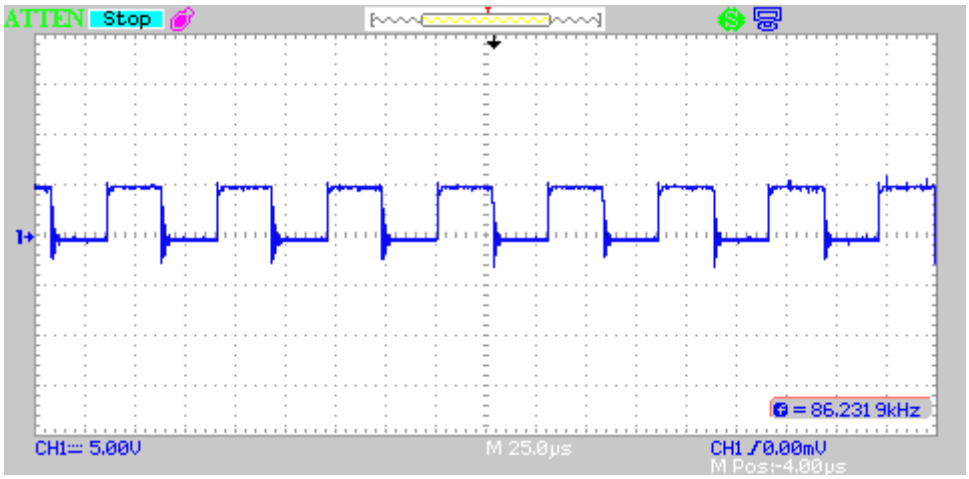


Figure 11: displays the results of an actual power switch duty cycle.

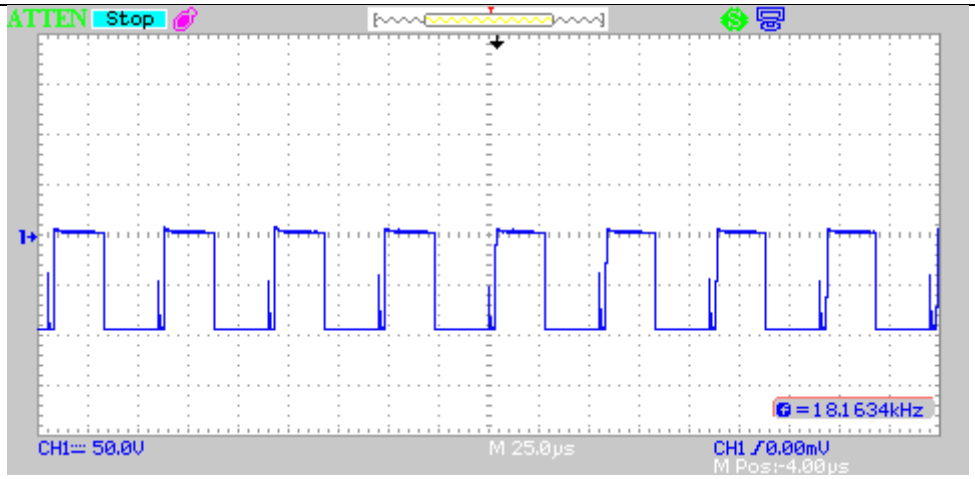
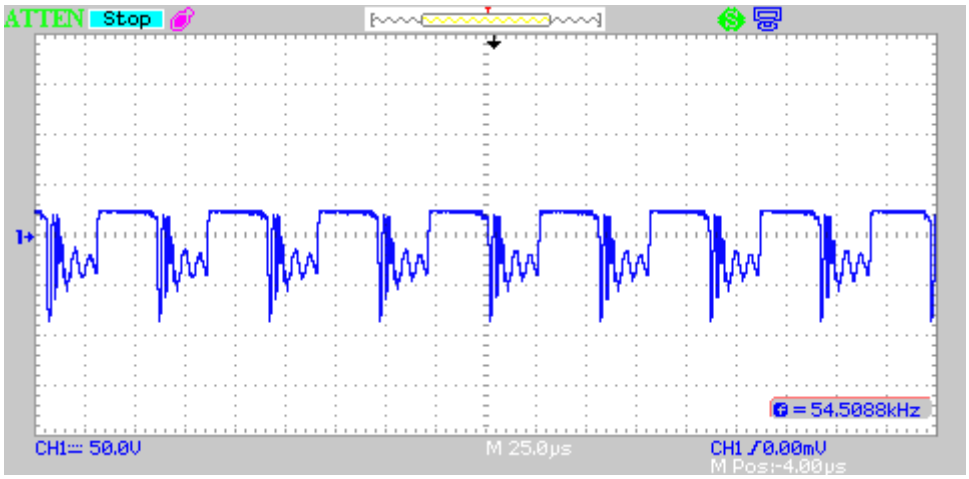
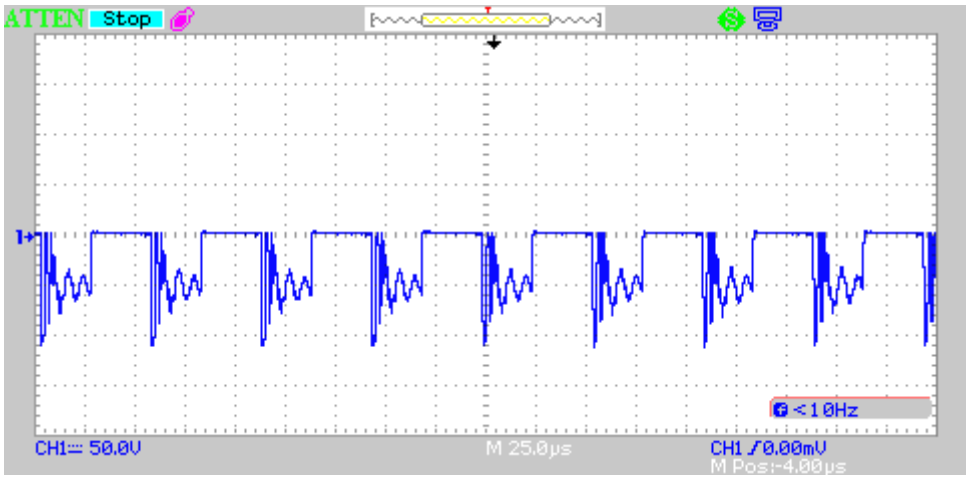


Figure 12: shows the voltage across the output diode as a function of time. (Do)



(Figure 13): The voltage across inductors as a consequence of the experiments (L1and L2)



(Figure 14) :shows people the voltage across a diode as a function of time (D1 and D2)

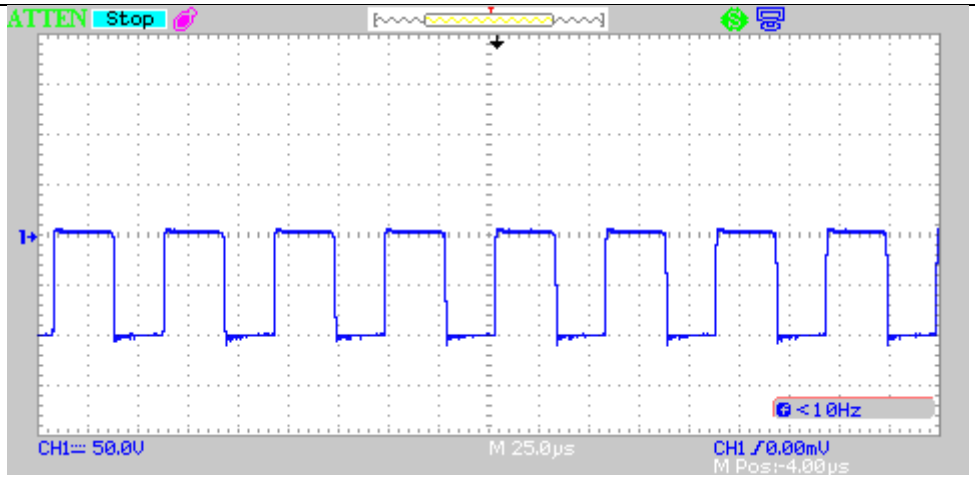


Fig. 15 shows the voltage across a diode after conducting experiments (D3)

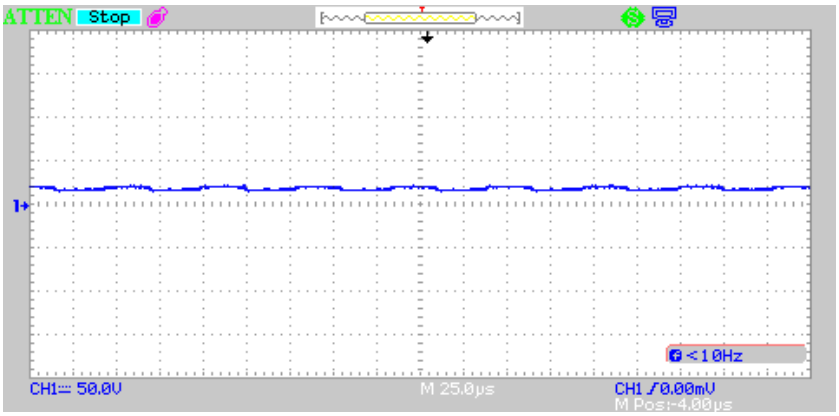


Figure 16 :shows the voltage across the capacitor as a function of time (C1 and C2)

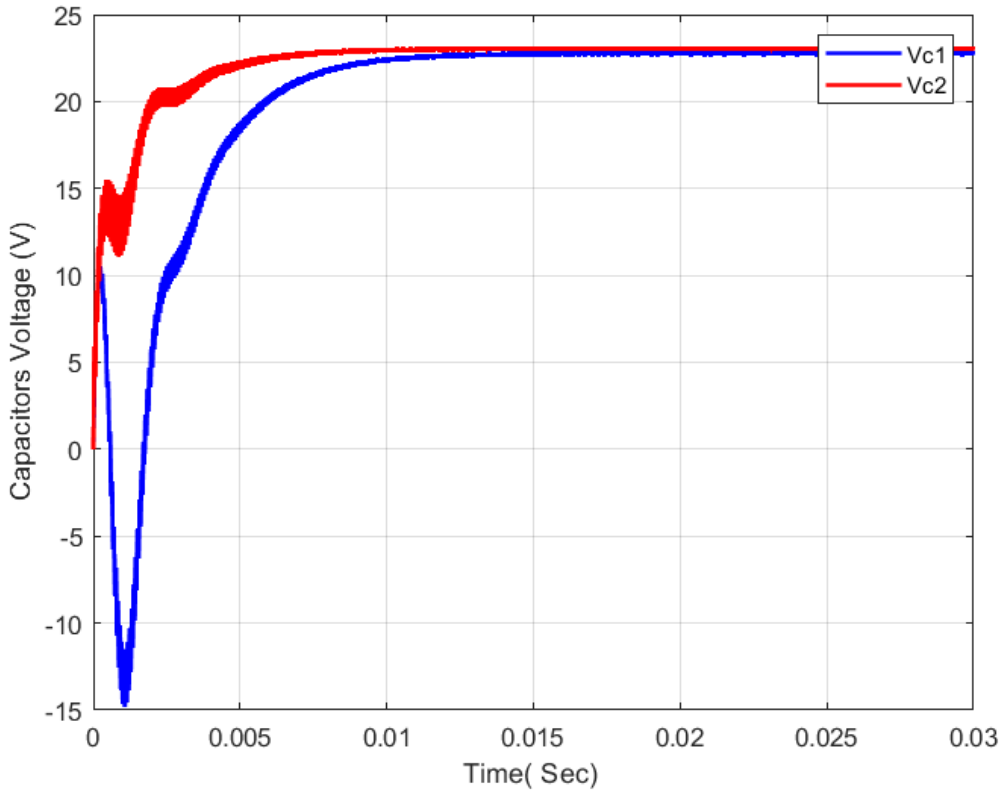


Figure (17). The Simulation Waveforms of voltage across capacitor (C1 and C2)for Converter

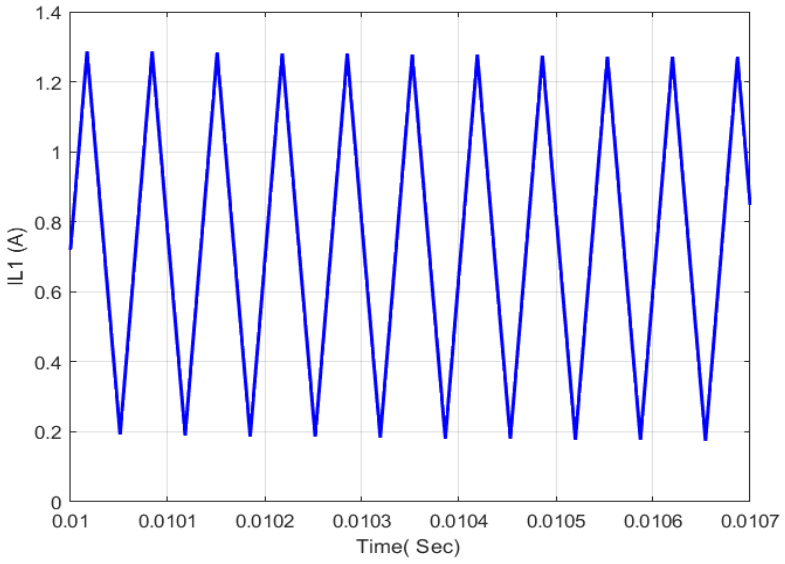


Figure (18). The Simulation Waveforms of Inductor Current for Converter

VIII. CONCLUSION

This study proposes a novel design and improved version of a modified converter based on the voltage lift cell.The suggested modification entails replacing the basic converter's switching inductor (SL) with a proposed inductor. In order to allow for an ultra-high rise in the voltage transfer ratio gain, a capacitor - inductor cell is used. Two inductors, two diodes, and one capacitor make up the hybrid switched capacitor - inductor cell. Furthermore, the new converter was developed, implemented, and tested in both CCM and DCM modes of operation. The suggested converters have a 95.6 percent efficiency. The end product isThe simulation, practical, and mathematically calculated equations all accord quite well. Using magnetically connected inductors and a diode-capacitor voltage multiplier, the converter's field of applicability may be expanded.

IX. REFERENCES

[1] Rashid, M.: 'Power electronics handbook' (Butterworth-Heinemann, 2011, 3rd edn.), pp. 265–356

[2] Luo, F.L., Ye, H.: 'Power electronics advanced DC/DC conversions technologies' (CRC Press, 2016), pp. 745p.

[3] Liangzong He and Wei Zhou 2015 High Step-up Active-Clamp Converter with an Input Current Doubler and a Symmetrical Switched-Capacitor Circuit *IEEE Transactions on Power Electronics* **24**(1),108–115. ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718 doi: org/10.6113/JPE.2015.15.3.587.

[4] Raghavendra, K.V.G., et al., "A Comprehensive Review of DC–DC Converter Topologies and Modulation Strategies with Recent Advances in Solar Photovoltaic Systems," *Electronics*, vol. 9, no. 1, pp. 1-41, 2020.

[5] Berkovich Y, Axelrod B, Madar R and Twina A 2015 Improved Luo converter modifications with increasing voltage ratio in *IET Power Electronics* **8**(2), pp. 202-212.

[6] Luo F, Ye H 2006 Essential DC/DC Converters. Boca Raton: CRC Press, https://doi.org/10.1201/9781420037104.

[7] Jiao Y P, Luo F L, and Zhu M 2011 Voltage-lift-type switched-inductor cells for enhancing dc-dc boost ability: principles and integrations in Luo converter *IET Power Electronics* **4**(1), pp. 131-142.

[8] Zhu M and Luo F L 2010 Enhanced self-lift Cûk converter for negative-topositive voltage conversion *IEEE Trans. Power Electron* **25**(9), pp. 2227-33.

[9] Axelrod B, Berkovich Y and Ioinovici A 2008 Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters. IEEE Transactions on Circuits and *Systems I: Regular Papers,* **55**(2), 687–696. doi:10.1109/tcsi.2008.916403.

[10] Hassan Jassim Motlak and Ahmed S. Rahi 2020 Performance comparison of different control strategies for the regulation of DC-DC negative output super-lift luo-converter", December 2020, pp. 5785~5792 , DOI: 10.11591/ijece.v10i6.pp5785-5792

[11] Zhu M and Luo F L 2010 Enhanced Self-Lift Cûk Converter for Negative-to-Positive Voltage Conversion. *IEEE Transactions on Power Electronics* **25**(9), 2227–33.

[12] Mohammadzadeh Shahir F, Babaei E and Farsadi M 2018 Voltage-Lift Technique Based Nonisolated Boost DC–DC Converter: Analysis and Design *IEEE Transactions on Power Electronics* **33**(7), 5917–26.

[13] Fang L L and Hong Y 2003 Positive output super-lift converters *IEEE Transactions on Power Electronics* **18**(1), 105–113.
[14] Jiao Y, Luo F L and Bose B K 2011 Voltage-lift split-inductor-type boost converters," in *IET Power Electronics* **4**(4), pp. 353-362.
[15] Yang L, Liang T and Chen J 2009 Transformerless DC–DC Converters With High Step-Up Voltage Gain in *IEEE Transactions on Industrial Electronics* **56**(8), pp. 3144-52.
[16] Axelrod B, Golan G, Berkovich Y and Shenkman A 2012 Diode–capacitor voltage multipliers combined with boost-converters: topologies and characteristics. *IET Power Electronics,* **5**(6), 873–884.
[17] Hwu K I, Chuang C F and Tu W C 2013 High Voltage-Boosting Converters Based on Bootstrap Capacitors and Boost Inductors. *IEEE Transactions on Industrial Electronics* **60**(6), 2178–93.
[18] Kevin Adrianto Nugraha and Tole Sutikno *2021 PID Control Based DC Boost Converter on Wheeled Soccer Robot*.Agustus 2021, pp. *BISTE Power Electronics,* 106-114 ISSN: 2685-9572.
[19] Tewari N and Sreedevi V T 2018 A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems. Solar Energy*,* **171***,* 466–477*.*
[20] Berkovich Y, Madar R, Axelrod B and Twina A 2015 Improved Luo converter modifications with increasing voltage ratio *IET Power Electronics* **8**(2), 202–212.