



## Research Article

# An Accurate and Fast Method for Improving ADC Nonlinearity

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Errors in analog-to-digital conversion (ADC) occur due to internal links or other electronic parts; faults that may occur during code conversion cannot be overlooked because signal digitalisation demands a large dynamic range and high resolution. This paper presents a new and accurate self-test method to compensate for one of the most effective errors of ADC because of its effect, which may result in a missing code, which is a differential nonlinear (DNL) of a 10-bit SAR-ADC. The proposed method includes three stages: DNL error modelling for nonideal system implementation, detection, and correction. To evaluate the proposed technique, sinusoidal and sawtooth signals are applied as analog inputs to the proposed system. Adaptivity, speed, and accuracy are the main motivations of this work, which provide high accuracy compared to other techniques, up to 9.6 ENOB and 59.2 SNR with sawtooth signal and 9.5 ENOB and 59.2 SNR with sinewave signals.

## 1. Introduction

A digital-to-analog converter (ADC) is an electrical component that converts analog signals to digital. ADCs are utilized in various applications, such as data collecting, signal processing, and control systems. However, in practical applications, their performance could be a lot better. The performance of ADCs and DACs substantially impacts many integrated circuits and systems. It can exhibit nonlinear behaviour in numerous applications such as signal processing, communications, instrumentation, and others for various reasons such as temperatures, component ageing, and manufacturing tolerances. These nonlinearities can cause conversion errors, impacting the measured data's accuracy. So, it must have acceptable linearity performance. As a result, all ADCs require accurate linearity testing periodically to validate the system [1]. ADC parameters are classified into static and dynamic categories [2].

One of the most important performance factors for ADCs is static nonlinearity, assessed in terms of integral nonlinearity (INL) and differential nonlinearity (DNL). The DNL is the deviation of the actual code width at each code

conversion from the ideal one least significant bit (LSB). A difference between the actual output codes and the ideal straight line is called an INL error [3]. The dynamic parameters are affected by the internal components, particularly the capacitor mismatch [4–6].

DNL and INL can be calculated using equations (1) and (5), respectively.

$$\text{DNL}(i) = \frac{(\text{WC}_{\text{LSB}})}{\text{LSB}}, \quad (1)$$

where WC is the code width given as  $\text{WC} = t(i+1) - t(i)$ .

$$\text{LSB} = \frac{\text{FSL}}{L}. \quad (2)$$

FS is the full scale of ADC voltage of ADC, and  $L$  is an ADC level which can be given by equation (4).

$$L = 2^N - 1, \quad (3)$$

$$\text{INL}(i) = \sum_{i=1}^k \text{DNL}. \quad (4)$$

Any behavioural model can provide a brief description of random errors such as noise, jitter, or glitches, as well as systematic errors (INL( $i$ ) and DNL( $i$ )) [7].

Figure 1 shows both DNL and INL errors with an ideal transition.

The main contributions of this article are as follows:

- (1) The proposition of the system can deal with a different input function
- (2) The suggestion of a new flexible method for error modelling is suitable for various error rates, sampling rates, and frequencies
- (3) System performance and resolution were enhanced (ENOB and SNR were improved)
- (4) Investigate a high accuracy compared to other works

## 2. Background

ADC parameters provide a proper impression of the performance of ADC in a particular application, such as the DNL. This is considered as a critical static parameter due to it causing missing code when the  $DNL \geq 1$  LSB; there is a possibility that the converter can become nonmonotonic. The code histogram test is an established technique for estimating these values [8]. The main weakness of the histogram method is the application's high cost, which is mostly caused by the need to obtain a high number of samples—more than a million—and the fact that this number generally rises exponentially with the ADC's bit count. These disadvantages make the histogram method impracticable for low-speed and high-resolution converters (>15 bits).

ADCs can be designed with built-in self-correction mechanisms to mitigate the effects of nonlinearities. First, it requires having an ideal ADC for comparison with a nonideal system. To achieve the nonideal system stage, errors must be added, either error added directly as a value from the datasheet or modelling an error. Nonideal ADC was modeled by MATLAB\Simulink R2021b software. ADS5400 parameter values were added directly by using a ramp function as the input signal [9]. The method's main disadvantage is that known error values are added for a specific type of input signal. Thus, it cannot be an adaptive practical method. Another behavioural modelling approach provides various nonidealities, such as clock jitter, clock feedthrough, and thermal and flicker noise, to the different blocks of the SAR-ADC [10]. A specific behavioural model based on the volterra series is proposed to describe the dynamic nonlinearities in time-interleaved analog-to-digital converter (TIADC) systems [11]. In this work, the error modelling method was applied in order to generate a DNL error, which will be used for proposed nonideal ADC modelling.

## 3. Proposed Methods

**3.1. Parameters Modelling.** With any ADC compensation error systems, parameters should first be described. The first stage of the proposed work is a DNL parameter modelling. According to the definitions of this parameter, the error modelling will present the impact of DNL on the output

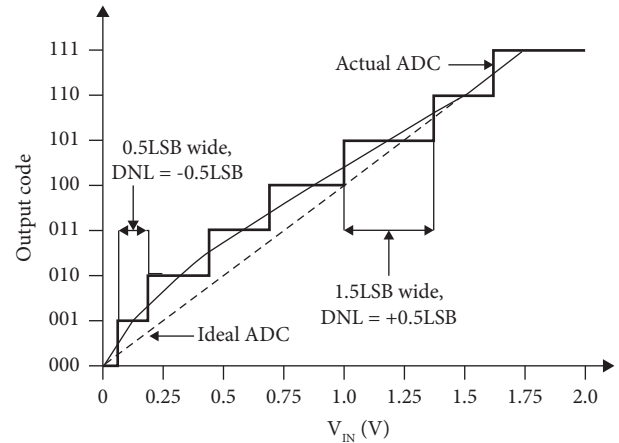


FIGURE 1: Ideal and actual ADC output affected by DNL and INL errors.

response that may generate a nonideal digital output transfer function step. This parameter directly affects the LSB by increasing or decreasing it from its normal value (+LSB%/−LSB%). To build an error modelling technique, we proposed a vector of length with the same length of input signal  $L$  faded to input signal including zeros and ones. In such a scenario, the LSB may be tuned by adding or subtracting the locations of one's present errors, which is randomly spread along the length with a variety of widths. Ideal sinusoidal and ramp input signals of a range of frequencies are applied, which will be affected by the errors that will change this system to nonideal ADC (NADC), as shown in Figure 2.

**3.2. Error Detection and Correction.** To achieve an accurate method of error detection and correction as a part of our proposed method, taking into account, the speed and simplicity of the method were considered. Several options were proposed, as listed in [12, 13].

The first step that should be followed for error correction methods is to use an ideal ADC that gives an ideal transfer function. Then, nonideal ADC is implemented by feeding a DNL error to the ideal signal as described in the last section, detecting the error location and then calculating the value of the error, which help to find the appropriate compensation method.

In [14], the built-in self-test (BIST) scheme was introduced based on the code width technique, which is used for error detection, and utilised a linear analog ramp signal applied to a 7-bit ADC flash type to create a digital sequence for testing. The curve fitting method is widely used to reduce purity requirements and decrease harmonic distortion and is considered an effective method to solve INL errors, as presented in [15, 16]. The nonlinear mismatch error calibration structure was included based on the sinusoidal wave fitting method used in [17, 18]. Adaptive least mean square (LMS) algorithms are used for nonlinear error extraction and calibration algorithms for pipeline ADC [19] to compensate for the gain error [20]. Kalman filter (KF) has been proposed as a resolution enhancement method [21]. Compared with the KF and adaptive-LMS method, the

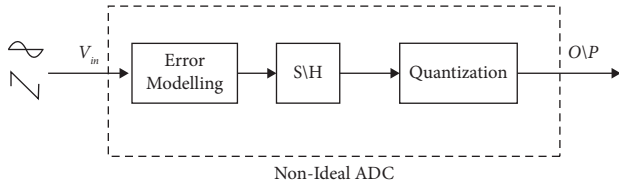


FIGURE 2: Nonideal ADC system.

output response of the proposed method provides a highly accurate result even when the error rate reaches to 0.1 of signal, which is more adaptive to different types of inputs and quickly checks the ADC under test performance, as will be illustrated in the next section.

Figures 3(a) and 3(b) describe the method presented in this paper. It mainly consists of two parts; the first one on the left refer to the proposed method of three stages: error modelling, detecting, and correcting stages. Second part includes an ideal ADC and its ideal outputs used in method evaluation.

The proposed method follows for nonideal system under test (NSUT) including the following points:

- (i) An ideal ADC (10-bit SAR-ADC) is initialized. The analog input signal of frequency ( $f$ ) was faded. For the method of evaluation, sinusoidal and sawtooth signals were used (10 KHz and 1 MHz) as a sampling frequency. Then, the ideal output response was collected.
- (ii) Error modelling stage was implemented by adding a vector of zeros with the same length ( $L$ ) (time of the signal); then, ones are distributed along this vector as a percentage of  $L$  with limited width so that a new LSB value will be ( $t\sim$ ).

$$t \sim (i) = t(i) + \frac{\sigma}{f \text{ sampling}}, \quad (5)$$

where  $\sigma$  is the LSB deviation, and then the error resulted was applied to the input signal as illustrated in Figure 4.

- (iii) Time shifting possibility of each step (LSB) was calculated using the following equation:

$$\text{shift} = t(i) - \text{LSB} * (i). \quad (6)$$

- (iv) Error detection stage is based on the location of the error being detected and the variety of LSB period time values being calculated, in equation (6).

At this stage, there is a threshold of error to occur, through which we can obtain an indication of the existence of the error.

- (v) Error correction: the extrapolation method is employed to estimate the true value after the error location has been determined.

## 4. Results and Discussion

Figure 5 shows the response of the KF method that was applied on a noisy sawtooth signal, which obviously reflects

the weakness of this method to process the nonlinearity of this signal type as illustrated.

Figures 6(a) and 6(b) present both noisy and corrected sine waves and sawtooth signals of 10 kHz as a sampling frequency and 0.1 as an error rate of DNL added to the ideal signal results from the proposed method which was the ideal SNR of 10-bit SAR-ADC equal to 61.96 dB.

Point (a) in Figure 6(a) shows how the transfer function of the sine wave signal was influenced by DNL error to give a nonideal transfer function of blue colour; DNL value at this point exceeds 1 LSB value; this clearly leads to missing code; also, it led to missing code in different steps on this transfer function as in point (c); the orange line of Figure 6(a) illustrates almost ideal transfer function results after applying the correction stage. The proposed effect is also clearly illustrated in Figure 6(b), when it is applied to sawtooth signal.

Figure 6 also shows the efficiency of the proposed method to handle the error that occurred even if 10% of the signal is influenced by the DNL error, still giving high resolution.

Figures 7(a) and 7(b) show the output response of (sampling frequency of 1 MHz and error rate of 0.1) sine wave and sawtooth signals.

Comparing the results of Figures 5, 6(b), and 7(b), we can see that the KF gives a weak response due to signal nonlinearity behaviour.

Also, as we can see, the noisy and corrected curves of sine and sawtooth signals give a clear impression about the efficiency of the proposed method even if the signal frequency and error rate are increased.

Figures 7(a), 7(b), 6(a), and 6(b) give an impression of how the affected steps are corrected to give an almost ideal step size equal to LSB (ideal step size).

DNL noise reduces the ADC resolution; this is clearly given in Tables 1–4 and how the ADC resolution improved with the corrected method.

To describe an ADC system's performance, the IEEE standard briefly describes the test methods and parameters [22]. A way of quantifying the quality of an ADC is known as the effective number of bit (EOB); a higher ENOB means that voltage levels recorded are more accurate as well as the signal-to-noise ratio (SNR). Both are calculated and considered the most important performance criteria of an ADC.

In this test, SNR calculation of an ideal digitalized sine wave and sawtooth signals separately was using the following equation:

$$\text{SNR} = 6.02 N + 1.76 \text{ dB}. \quad (7)$$

The fast Fourier transform (FFT) method is used to compute the SNR as a method that follows with a nonideal digitized.

Tables 1–3 briefly compare the collected data of the proposed method and Kalman method of parameters  $Q$  and  $R$ , and KF parameters are selected to provide best performance. The behavioural simulation results clearly verify the analysis's accuracy compared to the KF method. In addition,

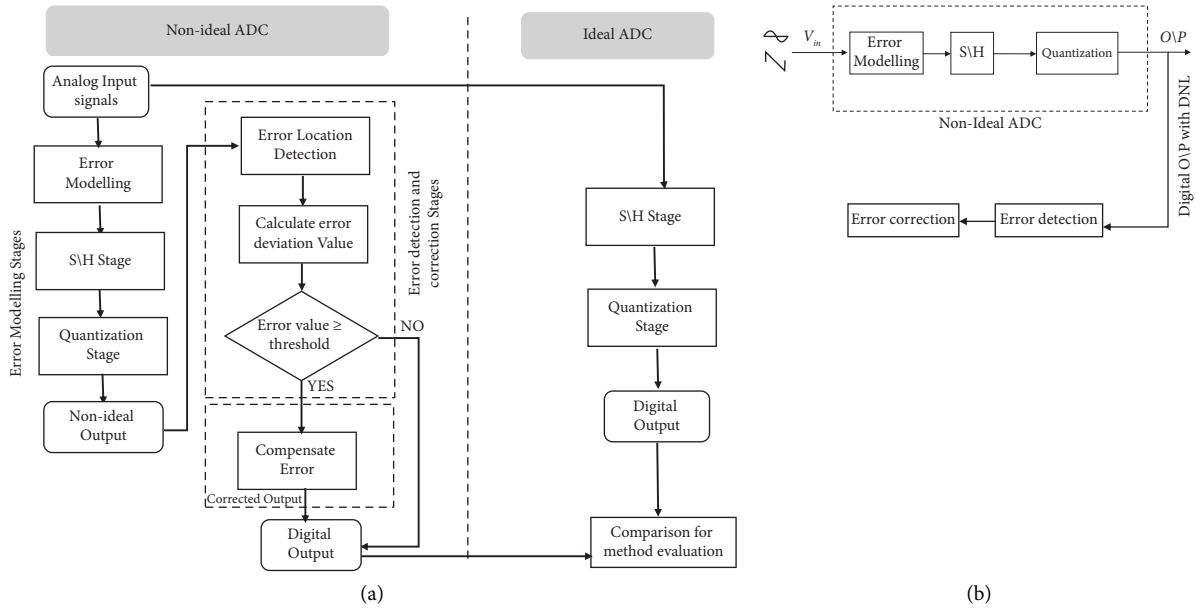


FIGURE 3: (a) Proposed method flowchart. (b) Block diagram.

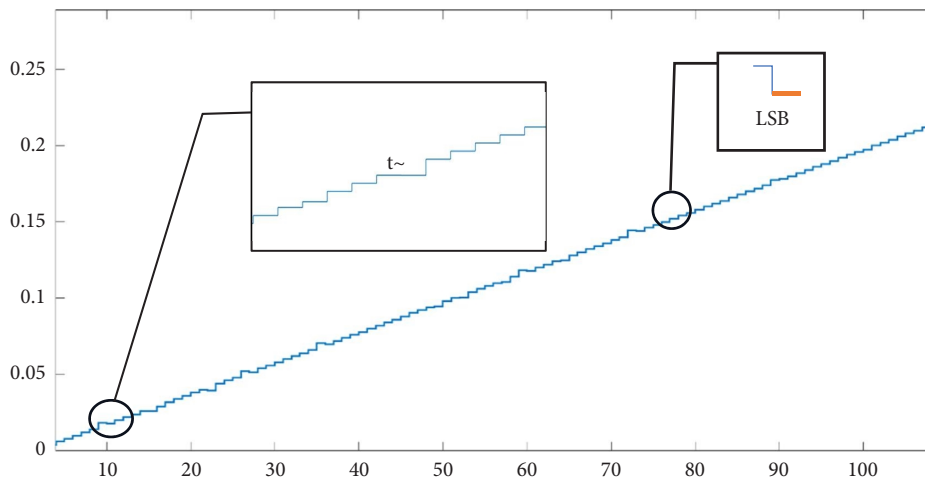


FIGURE 4: Nonideal transition line.

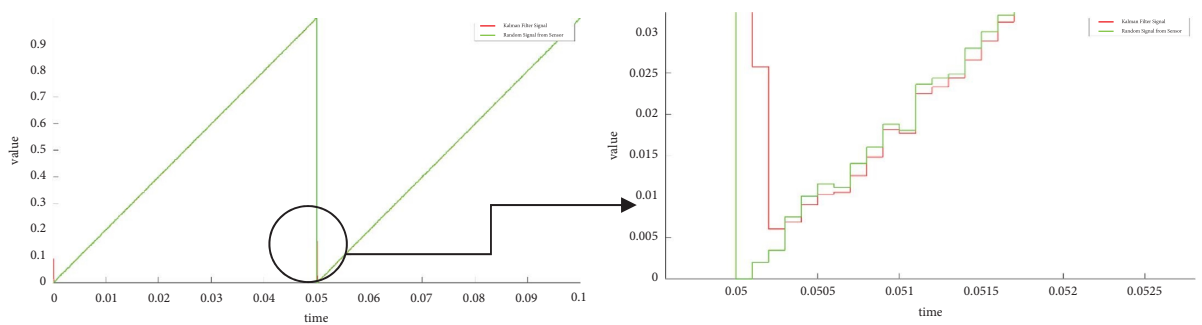


FIGURE 5: Noisy and corrected sawtooth signal of sampling frequency of 10 kHz and error rate of 0.01 using the Kalman filter.

KF has poor performance with ramp signals due to its nonlinearity; on the contrary, the proposed method maintains a high correction accuracy.

Table 4 gives a comparison between the proposed method and the adaptive-LMS method which was applied with the same environment; this method gives a better result

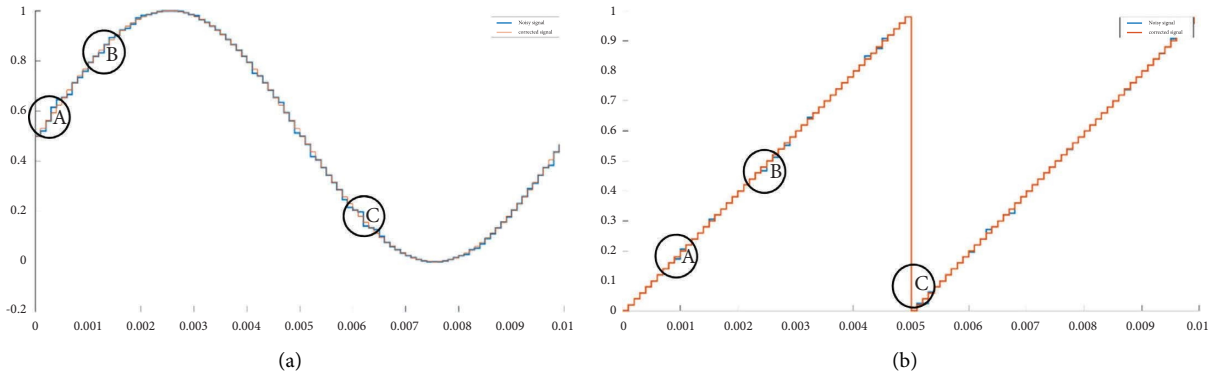


FIGURE 6: (a, b) Noisy and corrected sine and ramp signals (sampling frequency of 10kHz; error rate of 0.01).

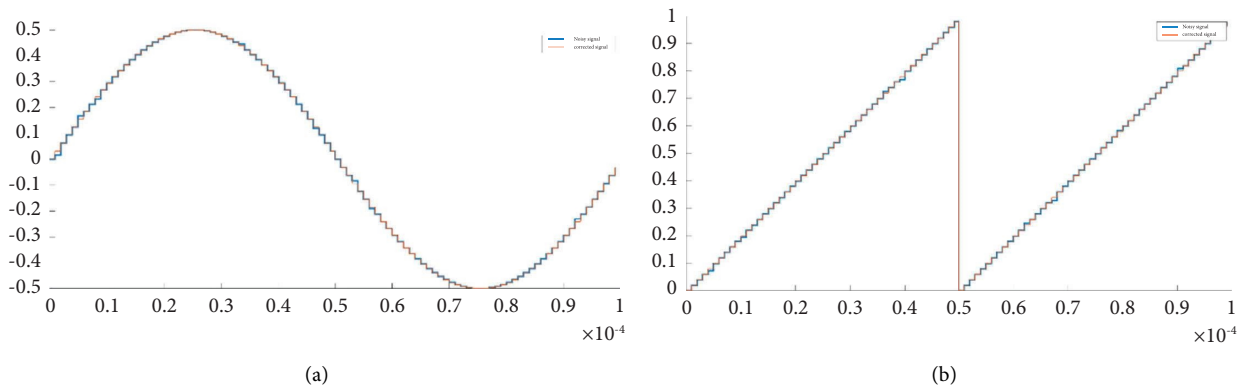


FIGURE 7: (a, b) Noisy and corrected sine and ramp signals (sampling frequency of 1 MHz; error rate of 0.1).

TABLE 1: Proposed method performance versus KF with sampling frequency of 10 kHz.

(Sampling frequency 10 kHz; error rate 0.01)									
Sawtooth					Sine wave				
Parameters	Kalman filter [19, 20]		Proposed algorithm		Kalman filter		Proposed algorithm		
	ENOB	SNR	ENOB	SNR	ENOB	SNR	ENOB	SNR	
Q	50								
R	15	7.2	45.3	9.5	59.6	9.2	57.3	9.5	59.2
Q	50								
R	5	6	37.9	9.6	58.7	9.4	58.8	9.5	59.2
Q	90								
R	20	6.3	39.9	9.5	58.7	9.3	58	9.5	59.1

TABLE 2: Proposed method performance versus KF with a sampling frequency of 1 MHz with 0.01 error rate.

(Sampling frequency 1 MHz; error rate 0.01)									
Sawtooth					Sine wave				
Parameters	Kalman filter [19, 20]		Proposed algorithm		Kalman filter		Proposed algorithm		
	ENOB	SNR	ENOB	SNR	ENOB	SNR	ENOB	SNR	
Q	50								
R	15	6	37.9	9.4	58.6	9.2	57.3	9.55	59.2
Q	50								
R	5	7.2	45.3	9.4	58.6	9.5	59	9.5	59.2
Q	90								
R	20	9.3	39.8	6.4	58.6	9.3	58	9.5	59.2

TABLE 3: Proposed method performance versus KF with a sampling frequency of 1 MHz with 0.1 error rate.

(Sampling frequency 1 MHz; error rate 0.1)									
Sawtooth					Sine wave				
Kalman filter [19, 20]		Proposed algorithm			Kalman filter		Proposed algorithm		
Parameters	ENOB	SNR	ENOB	SNR	ENOB	SNR	ENOB	SNR	
Q	50	6	37.9	9.4	58.6	9.2	57	9.52	59.1
R	15								
Q	50	7.2	45.2	9.4	58.2	9.4	58.4	9.52	59
R	5								
Q	90	6.3	39.3	9.4	58.5	9.2	57.6	9.5	58.9
R	20								

TABLE 4: Proposed method performance versus adaptive-LMS algorithm.

(Sampling frequency 1 MHz; error rate 0.1)									
Sawtooth					Sine wave				
LMS algorithm [17, 18]			Proposed algorithm		LMS algorithm		Proposed algorithm		
Parameters	ENOB	SNR	ENOB	SNR	ENOB	SNR	ENOB	SNR	
Sampling frequency	(1 MHz)	8.32	51.3	9.4	58.6	8.6	52.5	9.52	59.1
Error rate	0.1								
Sampling frequency	(10 kHz)	8.6	56	9.4	58.2	8.6	56.24	9.52	59
Error rate	0.01								

than KF but also still gives less performance than the suggested method, as shown the better performance reaches to 8.6 ENOB and 56.4 SNR with sinewave signal. In comparison, our method gives 9.52 ENOB and 59.1 SNR with a sinewave signal.

## 5. Conclusion

This paper presents a new and accurate ADC nonlinearity compensation technique. The proposed method was examined for 10-bit SAR-ADC to solve one of the most effective static parameters, DNL. The article focused on this parameter type due to its effect, which may cause missing code. The proposed technique was successfully tested by applying sinusoidal and sawtooth signals as inputs. The method includes three stages: error modelling with a new method, detection, and correction stage. The challenge was finding a method that maintains its efficiency even if the input signal was exposed to a high error rate and dealing with different signals of different frequencies, which was not included in previous work. The method provides improvement of ENOB and SNR performance up to 9.6 ENOB and 59.2 SNR with sawtooth signal and 9.5 ENOB 59.2 SNR compared with the Kalman filter-based system. When compared to adaptive-LMS, which obtained 8.6 ENOB and 56.24 SNR with sinusoidal input signal. The key benefits of the suggested strategy are flexibility, simplicity, efficiency, and speed, all achieved by this technique which makes it a more suitable for maintaining the ADC system.

## Data Availability

The data used to support the study are available from the corresponding author upon request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## References

- [1] H. Fan, "A bit cycling method for improving the DNL/INL in successive approximation register (SAR) analog-to-digital converter (ADC)," in *Proceedings of the 2018 New Generation of CAS (NGCAS)*, pp. 1–4, IEEE, Valletta, Malta, November 2018.
- [2] E. Alvarez-Fontecilla and A. Abusleme, "A non-linearity compensation technique for charge-redistribution sar adcs," in *Proceedings of the 2019 IEEE Latin American Test Symposium (LATS)*, pp. 1–4, IEEE, Santiago, Chile, March 2019.
- [3] J. V. R. Sp, "An ADC BIST using on-chip ramp generation and digital ORA," *Microelectronics Journal*, vol. 81, pp. 8–15, 2018.
- [4] N. Sun, "Error correction method of TIADC system based on parameter estimation of identification model," *Applied Sciences*, vol. 12, no. 12, p. 6257, 2022.
- [5] J. Wu, H. Xu, X. Cao, and T. Liu, "A 16-bit 120 MS/s pipelined ADC using a multi-level dither technique," *Electronics*, vol. 11, no. 23, p. 3979, 2022.
- [6] P. Bogner, *Gain Calibration for ADC with External Reference*, Google Patents, New York, NY, USA, 2017.
- [7] L. Michaeli and J. Šaliga, "Error models of the analog to digital converters," *Measurement Science Review*, vol. 14, no. 2, pp. 62–77, 2014.
- [8] A. Pavlidis, "SymBIST: symmetry-based analog and mixed-signal built-in self-test for functional safety," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2580–2593, 2021.
- [9] S. M. Taheri and B. Mohammadi, "Behavioral modelling of typical non-ideal analog to digital converter using MATLAB," *Transactions on Machine Learning and Artificial Intelligence*, vol. 2, no. 5, pp. 97–120, 2014.

- [10] S. Ahmed and V. Kakkar, "Modeling and simulation of an eight-bit auto-configurable successive approximation register analog-to-digital converter for cardiac and neural implants," *SIMULATION*, vol. 94, no. 1, pp. 11–29, 2018.
- [11] W. Wei, P. Ye, J. Song, H. Zeng, J. Gao, and Y. Zhao, "A behavioral dynamic nonlinear model for time-interleaved ADC based on volterra series," *IEEE Access*, vol. 7, pp. 41860–41873, 2019.
- [12] E. Balestrieri, P. Daponte, and S. Rapuano, "A state of the art on ADC error compensation methods," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 4, pp. 1388–1394, 2005.
- [13] A. Chakradhar, R. K. Srivastava, and S. R. Ijjada, "Calibration techniques of analog to digital converters (ADCs)," *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, pp. 415–419, 2019.
- [14] M. Senthil Sivakumar, T. Gurumekala, and S. Pulya, "Error detection of data conversion in flash ADC using code width based technique," *Procedia Computer Science*, vol. 165, pp. 270–277, 2019.
- [15] A. J. Gines, E. J. Peralias, and A. Rueda, "Black-box calibration for ADCs with hard nonlinear errors using a novel INL-based additive code: a pipeline ADC case study," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 7, pp. 1718–1729, 2017.
- [16] Z. Liang, D. Ren, J. Sun, and Z. Zhu, "Fitting algorithm of a sine wave with partial period waveforms and non-uniform sampling based on least-square method," *Journal of Physics: Conference Series*, vol. 1149, 2018, December.
- [17] J. Zhang, Y. Zhou, J. Zhao, G. Niu, and X. Luo, "Joint error estimation and calibration method of memory nonlinear mismatch for a four-channel 16-bit TIADC system," *Sensors*, vol. 22, no. 7, p. 2427, 2022.
- [18] Y. Zheng, Y. Zhao, N. Zhou, H. Wang, and D. Jiang, "A short review of some analog-to-digital converters resolution enhancement methods," *Measurement*, vol. 180, Article ID 109554, 2021.
- [19] J. Kaur, "Fast digital foreground gain error calibration for pipelined ADC," *IET Circuits, Devices and Systems*, vol. 13, no. 2, pp. 219–225, 2019.
- [20] T. Li, Y. Ni, Y. Zhang, and C. Chen, "LMS based ultra-fast non linearity test and calibration method for high-speed and high-resolution ADC," in *Proceedings of the 2021 IEEE 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, Xiamen, China, December 2021.
- [21] H. Hu, H. Shen, and Q. Pu, "Design and implementation of high-precision voltage measurement system based on Kalman filter and automatic calibration technology," *Measurement*, vol. 204, Article ID 112126, 2022.
- [22] S. J. Tilden, T. E. Linnenbrink, and P. J. Green, "Standard for terminology and test methods for analog-to-digital converters: a case study of utilization of IEEE-STD-1241," *Computer Standards & Interfaces*, vol. 22, no. 2, pp. 103–112, 2000.